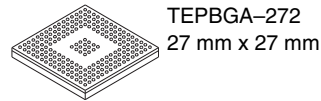


MPC5200B Data Sheet



Key features are shown below.

- MPC603e series e300 core
 - Superscalar architecture
 - 760 MIPS at 400 MHz (-40 to +85 °C)
 - 16 K-byte Instruction cache, 16 K-byte Data cache
 - Double precision FPU
 - Instruction and Data MMU
 - Standard and Critical interrupt capability
- SDRAM / DDR Memory Interface
 - up to 133-MHz operation
 - SDRAM and DDR SDRAM support
 - 256-MByte addressing range per CS, two CS available
 - 32-bit data bus
 - Built-in initialization and refresh
- Flexible multi-function External Bus Interface
 - Supports interfacing to ROM/Flash/SRAM memories or other memory mapped devices
 - 8 programmable Chip Selects
 - Non multiplexed data access using 8/16/32 bit databus with up to 26-bit address
 - Short or Long Burst capable
 - Multiplexed data access using 8/16/32 bit databus with up to 25-bit address
- Peripheral Component Interconnect (PCI) Controller
 - Version 2.2 PCI compatibility
 - PCI initiator and target operation
 - 32-bit PCI Address/Data bus
 - 33- and 66-MHz operation
 - PCI arbitration function
- ATA Controller
 - Version 4 ATA compatible external interface—IDE Disk Drive connectivity
- BestComm DMA subsystem
 - Intelligent virtual DMA Controller
 - Dedicated DMA channels to control peripheral reception and transmission
 - Local memory (SRAM 16 kBytes)
- 6 Programmable Serial Controllers (PSC)
 - UART or RS232 interface
 - CODEC interface for Soft Modem, Master/Slave CODEC Mode, I²S and AC97
- Full duplex SPI mode
- IrDA mode from 2400 bps to 4 Mbps
- Fast Ethernet Controller (FEC)
 - Supports 100Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII, 10 Mbps 7-wire interface
- Universal Serial Bus Controller (USB)
 - USB Revision 1.1 Host
 - Open Host Controller Interface (OHCI)
 - Integrated USB Hub, with two ports.
- Two Inter-Integrated Circuit Interfaces (I²C)
- Serial Peripheral Interface (SPI)
- Dual CAN 2.0 A/B Controller (MSCAN)
 - Implementation of version 2.0A/B CAN protocol
 - Standard and extended data frames
- J1850 Byte Data Link Controller (BDLC)
- J1850 Class B data communication network interface compatible and ISO compatible for low speed (<125 kbps) serial data communications in automotive applications.
- Supports 4X mode, 41.6 kbps
- In-frame response (IFR) types 0, 1, 2, and 3 supported
- Systems level features
 - Interrupt Controller supports four external interrupt request lines and 47 internal interrupt sources
 - GPIO/Timer functions
Up to 56 total GPIO pins that support a variety of interrupt/WakeUp capabilities.
Eight GPIO pins with timer capability supporting input capture, output compare, and pulse width modulation (PWM) functions
 - Real-time Clock with one-second resolution
 - Systems Protection (watch dog timer, bus monitor)
 - Individual control of functional block clock sources
 - Power management: Nap, Doze, Sleep, Deep Sleep modes
 - Support of WakeUp from low power modes by different sources (GPIO, RTC, CAN)
- Test/Debug features
 - JTAG (IEEE 1149.1 test access port)
 - Common On-chip Processor (COP) debug port
- On-board PLL and clock generation

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Figure 1 shows a simplified MPC5200B block diagram.

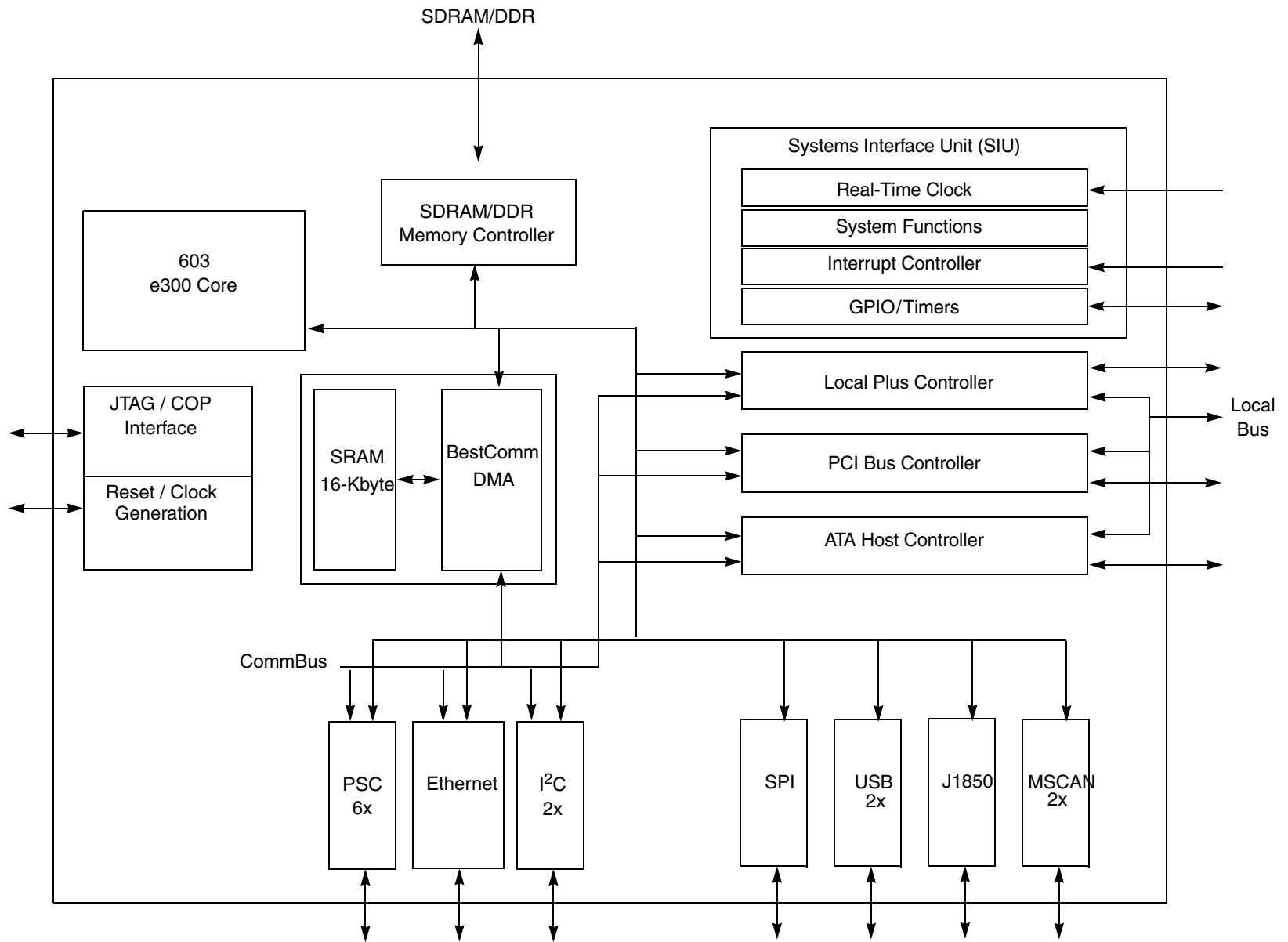


Figure 1. Simplified Block Diagram—MPC5200B

1 Electrical and Thermal Characteristics

1.1 DC Electrical Characteristics

1.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5200B DC Electrical characteristics. [Table 1](#) gives the absolute maximum ratings.

Table 1. Absolute Maximum Ratings⁽¹⁾

| Characteristic | Sym | Min | Max | Unit | SpecID |
|---|-----------------------|------|---------------------|------|--------|
| Supply voltage - e300 core and peripheral logic | VDD_CORE | -0.3 | 1.8 | V | D1.1 |
| Supply voltage - I/O buffers | VDD_IO, VDD_MEM_IO | -0.3 | 3.6 | V | D1.2 |
| Supply voltage - System APLL | SYS_PLL_AVDD | -0.3 | 2.1 | V | D1.3 |
| Supply voltage - e300 APLL | CORE_PLL_AVDD | -0.3 | 2.1 | V | D1.4 |
| Input voltage (VDD_IO) | V _{in} | -0.3 | VDD_IO + 0.3 | V | D1.5 |
| Input voltage (VDD_MEM_IO) | V _{in} | -0.3 | VDD_MEM_IO + 0.3 | V | D1.6 |
| Input voltage overshoot | V _{inos} | - | 1.0 | V | D1.7 |
| Input voltage undershoot | V _{inus} | - | 1.0 | V | D1.8 |
| Storage temperature range | T _{stg} | -55 | 150 | °C | D1.9 |

¹ Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

1.1.2 Recommended Operating Conditions

[Table 2](#) gives the recommended operating conditions.

Table 2. Recommended Operating Conditions

| Characteristic | Sym | Min ⁽¹⁾ | Max ⁽¹⁾ | Unit | SpecID |
|---|---------------------------|--------------------|--------------------|------|--------|
| Supply voltage - e300 core and peripheral logic | VDD_CORE | 1.42 | 1.58 | V | D2.1 |
| Supply voltage - standard I/O buffers | VDD_IO | 3.0 | 3.6 | V | D2.2 |
| Supply voltage - memory I/O buffers (SDR) | VDD_MEM_IO _{SDR} | 3.0 | 3.6 | V | D2.3 |
| Supply voltage - memory I/O buffers (DDR) | VDD_MEM_IO _{DDR} | 2.42 | 2.63 | V | D2.4 |
| Supply voltage - System APLL | SYS_PLL_AVDD | 1.42 | 1.58 | V | D2.5 |
| Supply voltage - e300 APLL | CORE_PLL_AVDD | 1.42 | 1.58 | V | D2.6 |

Table 2. Recommended Operating Conditions (continued)

| Characteristic | Sym | Min ⁽¹⁾ | Max ⁽¹⁾ | Unit | SpecID |
|--|--------------------|--------------------|---------------------------|------|--------|
| Input voltage - standard I/O buffers | V _{in} | 0 | VDD_IO | V | D2.7 |
| Input voltage - memory I/O buffers (SDR) | V _{inSDR} | 0 | VDD_MEM_IO _{SDR} | V | D2.8 |
| Input voltage - memory I/O buffers (DDR) | V _{inDDR} | 0 | VDD_MEM_IO _{DDR} | V | D2.9 |
| Ambient operating temperature range ⁽²⁾ | T _A | -40 | +85 | °C | D2.10 |
| Die junction operating temperature range | T _j | -40 | +115 | °C | D2.12 |

¹ These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

² Maximum e300 core operating frequency is 400 MHz

1.1.3 DC Electrical Specifications

Table 3 gives the DC Electrical characteristics for the MPC5200B at recommended operating conditions (see Table 2).

Table 3. DC Electrical Specifications

| Characteristic | Condition | Sym | Min | Max | Unit | SpecID |
|-----------------------|---|------------------|-----|-----|------|--------|
| Input high voltage | Input type = TTL VDD_IO/VDD_MEM_IO _{SDR} | V _{IH} | 2.0 | — | V | D3.1 |
| Input high voltage | Input type = TTL VDD_MEM_IO _{DDR} | V _{IH} | 1.7 | — | V | D3.2 |
| Input high voltage | Input type = PCI VDD_IO | V _{IH} | 2.0 | — | V | D3.3 |
| Input high voltage | Input type = SCHMITT VDD_IO | V _{IH} | 2.0 | — | V | D3.4 |
| Input high voltage | SYS_XTAL_IN | CV _{IH} | 2.0 | — | V | D3.5 |
| Input high voltage | RTC_XTAL_IN | CV _{IH} | 2.0 | — | V | D3.6 |
| Input low voltage | Input type = TTL VDD_IO/VDD_MEM_IO _{SDR} | V _{IL} | — | 0.8 | V | D3.7 |
| Input low voltage | Input type = TTL VDD_MEM_IO _{DDR} | V _{IL} | — | 0.7 | V | D3.8 |
| Input low voltage | Input type = PCI VDD_IO | V _{IL} | — | 0.8 | V | D3.9 |
| Input low voltage | Input type = SCHMITT VDD_IO | V _{IL} | — | 0.8 | V | D3.10 |
| Input low voltage | SYS_XTAL_IN | CV _{IL} | — | 0.8 | V | D3.11 |
| Input low voltage | RTC_XTAL_IN | CV _{IL} | — | 0.8 | V | D3.12 |
| Input leakage current | V _{in} = 0 or VDD_IO/VDD_IO_MEM _{SDR} (depending on input type ⁽¹⁾) | I _{IN} | — | ±2 | μA | D3.13 |
| Input leakage current | SYS_XTAL_IN V _{in} = 0 or VDD_IO | I _{IN} | — | ±10 | μA | D3.14 |

Table 3. DC Electrical Specifications (continued)

| Characteristic | Condition | Sym | Min | Max | Unit | SpecID |
|--|---|--------------------|------|-----|------|--------|
| Input leakage current | RTC_XTAL_IN Vin = 0 or VDD_IO | I _{IN} | — | ±10 | μA | D3.15 |
| Input current, pullup resistor | PULLUP VDD_IO Vin = 0 | I _{INpu} | 40 | 109 | μA | D3.16 |
| Input current, pullup resistor - memory I/O buffers | PULLUP_MEM VDD_IO_MEM _{SDR} Vin = 0 | I _{INpu} | 41 | 111 | μA | D3.17 |
| Input current, pulldown resistor | PULLDOWN VDD_IO Vin = VDD_IO | I _{INpd} | 36 | 106 | μA | D3.18 |
| Output high voltage | IOH is driver dependent ⁽²⁾ VDD_IO, VDD_IO_MEM _{SDR} | V _{OH} | 2.4 | — | V | D3.19 |
| Output high voltage | IOH is driver dependent ⁽²⁾ VDD_IO_MEM _{DDR} | V _{OHDDR} | 1.7 | — | V | D3.20 |
| Output low voltage | IOL is driver dependent ⁽²⁾ VDD_IO, VDD_IO_MEM _{SDR} | V _{OL} | — | 0.4 | V | D3.21 |
| Output low voltage | IOL is driver dependent ⁽²⁾ VDD_IO_MEM _{DDR} | V _{OLDDR} | — | 0.4 | V | D3.22 |
| DC Injection Current Per Pin ⁽³⁾ | | I _{CS} | -1.0 | 1.0 | mA | D3.23 |
| Capacitance | Vin = 0V, f = 1 MHz | C _{in} | — | 15 | pF | D3.24 |

¹ Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

² See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.

³ All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range. Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 4. Drive Capability of MPC5200B Output Pins

| Driver Type | Supply Voltage | I _{OH} | I _{OL} | Unit | SpecID |
|-------------|-------------------|-----------------|-----------------|------|--------|
| DRV4 | VDD_IO = 3.3V | 4 | 4 | mA | D3.25 |
| DRV8 | VDD_IO = 3.3V | 8 | 8 | mA | D3.26 |
| DRV8_OD | VDD_IO = 3.3V | - | 8 | mA | D3.27 |
| DRV16_MEM | VDD_IO_MEM = 3.3V | 16 | 16 | mA | D3.28 |
| DRV16_MEM | VDD_IO_MEM = 2.5V | 16 | 16 | mA | D3.29 |
| PCI | VDD_IO = 3.3V | 16 | 16 | mA | D3.30 |

1.1.4 Electrostatic Discharge

CAUTION

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (GND or V_{CC}). Table 7 gives package thermal characteristics for this device.

Table 5. ESD and Latch-Up Protection Characteristics

| Sym | Rating | Min | Max | Unit | SpecID |
|-----------|--|--------------|-----|------|--------|
| V_{HBM} | Human Body Model (HBM)—JEDEC JESD22-A114-B | 2000 | — | V | D4.1 |
| V_{MM} | Machine Model (MM)—JEDEC JESD22-A115 | 200 | — | V | D4.2 |
| V_{CDM} | Charge Device Model (CDM)—JEDEC JESD22-C101 | 500 | — | V | D4.3 |
| I_{LAT} | Latch-up Current at $T_A=85^\circ\text{C}$ positive negative | +100 -100 | — | mA | D4.4 |
| I_{LAT} | Latch-up Current at $T_A=27^\circ\text{C}$ positive negative | +200 -200 | — | mA | D4.5 |

1.1.5 Power Dissipation

Power dissipation of the MPC5200B is caused by 3 different components: the dissipation of the internal or core digital logic (supplied by VDD_{CORE}), the dissipation of the analog circuitry (supplied by SYS_PLL_AVDD and $CORE_PLL_AVDD$) and the dissipation of the IO logic (supplied by VDD_{IO_MEM} and VDD_{IO}). Table 6 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins can not be given in general, but must be calculated by the user for each application case using the following formula:

$$P_{IO} = P_{IOint} + \sum_M N \times C \times VDD_{IO}^2 \times f \quad \text{Eqn. 1}$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, VDD_{IO} is the IO voltage swing, f is the switching frequency and P_{IOint} is the power consumed by the unloaded IO stage. The total power consumption of the MPC5200B processor must not exceed the value, which would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{analog} + P_{IO} \quad \text{Eqn. 2}$$

Table 6. Power Dissipation

| Core Power Supply (VDD_CORE) | | | | | SpecID |
|--|---------------------------------|-------------------|------|---------|--------|
| Mode | SYS_XTAL/XLB/PCI/IPB/CORE (MHz) | | Unit | Notes | |
| | 33/66/33/33/264 | 33/132/66/132/396 | | | |
| | Typ | Typ | | | |
| Operational | 727.5 | 1080 | mW | (1),(2) | D5.1 |
| Doze | — | 600 | mW | (1),(3) | D5.2 |
| Nap | — | 225 | mW | (1),(4) | D5.3 |
| Sleep | — | 225 | mW | (1),(5) | D5.4 |
| Deep-Sleep | 52.5 | 52.5 | mW | (1),(6) | D5.5 |
| PLL Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD) | | | | | |
| Mode | Typ | | Unit | Notes | |
| Typical | 2 | | mW | (7) | D5.6 |
| Unloaded I/O Power Supplies (VDD_IO, VDD_MEM_IO ⁸) | | | | | |
| Mode | Typ | | Unit | Notes | |
| Typical | 33 | | mW | (9) | D5.7 |

¹ Typical core power is measured at VDD_CORE = 1.5 V, Tj = 25 C

² Operational power is measured while running an entirely cache-resident program with floating-point multiplication instructions in parallel with a continuous PCI transaction via BestComm.

³ Doze power is measured with the e300 core in Doze mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

⁴ Nap power is measured with the e300 core in Nap mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

⁵ Sleep power is measured with the e300 core in Sleep mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

⁶ Deep-Sleep power is measured with the e300 core in Sleep mode, the system oscillator, System PLL, Core PLL and all other system modules are inactive

⁷ Typical PLL power is measured at SYS_PLL_AVDD = CORE_PLL_AVDD = 1.5 V, Tj = 25 C

⁸ IO power figures given in the table represent the worst case scenario. For the VDD_MEM_IO rail connected to 2.5V the IO power is expected to be lower and bounded by the worst case with VDD_MEM_IO connected to 3.3V.

⁹ Unloaded typical I/O power is measured in Deep-Sleep mode at VDD_IO = VDD_MEM_IO_{SDR} = 3.3 V, Tj = 25 C

1.1.6 Thermal Characteristics

Table 7. Thermal Resistance Data

| Rating | Board Layers | Sym | Value | Unit | Notes | SpecID |
|--|-------------------------|------------------|-------|------|---------|--------|
| Junction to Ambient Natural Convection | Single layer board (1s) | $R_{\theta JA}$ | 30 | °C/W | (1),(2) | D6.1 |
| Junction to Ambient Natural Convection | Four layer board (2s2p) | $R_{\theta JMA}$ | 22 | °C/W | (1),(3) | D6.2 |
| Junction to Ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 24 | °C/W | (1),(3) | D6.3 |
| Junction to Ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 19 | °C/W | (1),(3) | D6.4 |
| Junction to Board | — | $R_{\theta JB}$ | 14 | °C/W | (4) | D6.5 |
| Junction to Case | — | $R_{\theta JC}$ | 8 | °C/W | (5) | D6.6 |
| Junction to Package Top | Natural Convection | Ψ_{JT} | 2 | °C/W | (6) | D6.7 |

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

1.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J , can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ = junction to case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package ($^{\circ}\text{C}$)

Ψ_{JT} = thermal characterization parameter ($^{\circ}\text{C}/\text{W}$)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

1.2 Oscillator and PLL Electrical Characteristics

The MPC5200B System requires a system-level clock input SYS_XTAL. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200B clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

1.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

| Characteristic | Sym | Notes | Min | Typical | Max | Unit | SpecID |
|--------------------------|------------------------|-------|------|---------|------|------|--------|
| SYS_XTAL frequency | $f_{\text{sys_xtal}}$ | | 15.6 | 33.3 | 35.0 | MHz | O1.1 |
| Oscillator start-up time | $t_{\text{up_osc}}$ | | — | — | 10 | ms | O1.2 |

1.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

| Characteristic | Sym | Notes | Min | Typical | Max | Unit | SpecID |
|--------------------|------------------------|-------|-----|---------|-----|------|--------|
| RTC_XTAL frequency | $f_{\text{rtc_xtal}}$ | | — | 32.768 | — | kHz | O2.1 |

1.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

| Characteristic | Sym | Notes | Min | Typical | Max | Unit | SpecID |
|-----------------------------|------------------------|-------|------|---------|------|---------------|--------|
| SYS_XTAL frequency | $f_{\text{sys_xtal}}$ | (1) | 15.6 | 33.3 | 35.0 | MHz | O3.1 |
| SYS_XTAL cycle time | $t_{\text{sys_xtal}}$ | (1) | 66.6 | 30.0 | 28.5 | ns | O3.2 |
| SYS_XTAL clock input jitter | t_{jitter} | (2) | — | — | 150 | ps | O3.3 |
| System VCO frequency | f_{VCOsys} | (1) | 250 | 533 | 800 | MHz | O3.4 |
| System PLL relock time | t_{lock} | (3) | — | — | 100 | μs | O3.5 |

¹ The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

² This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.

³ Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

1.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 11. e300 PLL Specifications

| Characteristic | Sym | Notes | Min | Typical | Max | Unit | SpecID |
|-----------------------------|-----------------------|-------|------|---------|------|---------------|--------|
| e300 frequency | f_{core} | (1) | 50 | — | 550 | MHz | O4.1 |
| e300 cycle time | t_{core} | (1) | 2.85 | — | 40.0 | ns | O4.2 |
| e300 VCO frequency | f_{VCOcore} | (1) | 400 | — | 1200 | MHz | O4.3 |
| e300 input clock frequency | $f_{\text{XLB_CLK}}$ | | 25 | — | 367 | MHz | O4.4 |
| e300 input clock cycle time | $t_{\text{XLB_CLK}}$ | | 2.73 | — | 50.0 | ns | O4.5 |
| e300 input clock jitter | t_{jitter} | (2) | — | — | 150 | ps | O4.6 |
| e300 PLL relock time | t_{lock} | (3) | — | — | 100 | μs | O4.7 |

¹ The XLB_CLK frequency and e300 PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and e300 PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies in [Table 12](#).

² This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.

³ Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

1.3 AC Electrical Characteristics

Hyperlinks to the indicated timing specification sections are provided below.

- [AC Operating Frequency Data](#)
- [Clock AC Specifications](#)
- [Resets](#)
- [External Interrupts](#)
- [SDRAM](#)
- [PCI](#)
- [Local Plus Bus](#)
- [ATA](#)
- [Ethernet](#)
- [USB](#)
- [SPI](#)
- [MSCAN](#)
- [I²C](#)
- [J1850](#)
- [PSC](#)
- [GPIOs and Timers](#)
- [IEEE 1149.1 \(JTAG\) AC Specifications](#)

1.3.1 AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

- TA = -40 to 85 °C
- Tj = -40 to 115 °C
- VDD_CORE = 1.42 to 1.58 V
VDD_IO = 3.0 to 3.6 V

- Input conditions:
All Inputs: $t_r, t_f \leq 1$ ns
- Output Loading:
All Outputs: 50 pF

1.3.2 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200B.

Table 12. Clock Frequencies

| | | Min | Max | Units | SpecID |
|---|----------------------------|------|-----|-------|--------|
| 1 | e300 Processor Core | — | 400 | MHz | A1.1 |
| 2 | SDRAM Clock | — | 133 | MHz | A1.2 |
| 3 | XL Bus Clock | — | 133 | MHz | A1.3 |
| 4 | IP Bus Clock | — | 133 | MHz | A1.4 |
| 5 | PCI / Local Plus Bus Clock | — | 66 | MHz | A1.5 |
| 6 | PLL Input Range | 15.6 | 35 | MHz | A1.6 |

1.3.3 Clock AC Specifications

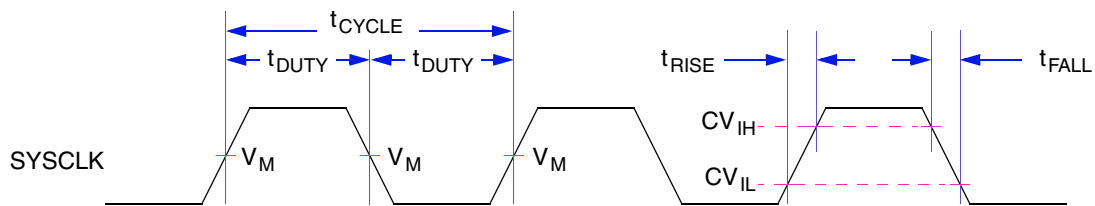


Figure 2. Timing Diagram—SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

| Sym | Description | Min | Max | Units | SpecID |
|-------------|---|------|------|-------|--------|
| t_{CYCLE} | SYS_XTAL_IN cycle time. ⁽¹⁾ | 28.6 | 64.1 | ns | A2.1 |
| t_{RISE} | SYS_XTAL_IN rise time. | — | 5.0 | ns | A2.2 |
| t_{FALL} | SYS_XTAL_IN fall time. | — | 5.0 | ns | A2.3 |
| t_{DUTY} | SYS_XTAL_IN duty cycle (measured at V_M). ⁽²⁾ | 40.0 | 60.0 | % | A2.4 |
| CV_{IH} | SYS_XTAL_IN input voltage high | 2.0 | — | V | A2.5 |
| CV_{IL} | SYS_XTAL_IN input voltage low | — | 0.8 | V | A2.6 |

¹ **CAUTION**—The SYS_XTAL_IN frequency and system PLL_CFG[0-6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the MPC5200B User Manual.

² SYS_XTAL_IN duty cycle is measured at V_M .

1.3.4 Resets

The MPC5200B has three reset pins:

- $\overline{\text{PORRESET}}$ - Power on Reset
- $\overline{\text{HRESET}}$ - Hard Reset
- $\overline{\text{SRESET}}$ - Software Reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5200B inputs, as specified in the DC Electrical Specifications section. Table 14 specifies the pulse widths of the Reset inputs.

Table 14. Reset Pulse Width

| Name | Description | Min Pulse Width | Max Pulse Width | Reference Clock | SpecID |
|----------|----------------|---|-----------------|-----------------|--------|
| PORRESET | Power On Reset | $t_{\text{VDD_stable}} + t_{\text{up_osc}} + t_{\text{lock}}$ | — | SYS_XTAL_IN | A3.1 |
| HRESET | Hardware Reset | 4 clock cycles | — | SYS_XTAL_IN | A3.2 |
| SRESET | Software Reset | 4 clock cycles | — | SYS_XTAL_IN | A3.3 |

For $\overline{\text{PORRESET}}$ the value of the minimum pulse width reflects the power on sequence. If $\overline{\text{PORRESET}}$ is asserted afterwards its minimum pulse width equals the minimum given for $\overline{\text{HRESET}}$ related to the same reference clock.

The $t_{\text{VDD_stable}}$ describes the time which is needed to get all power supplies stable.

For t_{lock} , refer to the Oscillator/PLL section of this specification for further details.

For $t_{\text{up_osc}}$, refer to the Oscillator/PLL section of this specification for further details.

Following the deassertion of $\overline{\text{PORRESET}}$, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ remain low for 4096 reference clock cycles.

The deassertion of $\overline{\text{HRESET}}$ for at least the minimum pulse width forces the internal resets to be active for an additional 4096 clock cycles.

NOTE

As long as VDD is not stable the $\overline{\text{HRESET}}$ output is not stable.

Table 15. Reset Rise/Fall Timing

| Description | Min | Max | Unit | SpecID |
|--|-----|-----|------|--------|
| $\overline{\text{PORRESET}}$ fall time | — | 1 | ms | A3.4 |
| $\overline{\text{PORRESET}}$ rise time | — | 1 | ms | A3.5 |
| $\overline{\text{HRESET}}$ fall time | — | 1 | ms | A3.6 |
| $\overline{\text{HRESET}}$ rise time | — | 1 | ms | A3.7 |
| $\overline{\text{SRESET}}$ fall time | — | 1 | ms | A3.8 |
| $\overline{\text{SRESET}}$ rise time | — | 1 | ms | A3.9 |

NOTE

Make sure that the $\overline{\text{PORRESET}}$ does not carry any glitches. The MPC5200B has no filter to prevent them from getting into the chip. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ must have a monotonous rise time. The assertion of $\overline{\text{HRESET}}$ becomes active at Power on Reset without any SYS_XTAL clock.

For additional information, see the MPC5200B User Manual.

1.3.4.1 Reset Configuration Word

During reset ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) the Reset Configuration Word is latched in the related Reset Configuration Word Register with each rising edge of the SYS_XTAL signal. If both resets ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) are inactive (high), the contents of this register are locked immediately with the SYS_XTAL clock (see Figure 3).

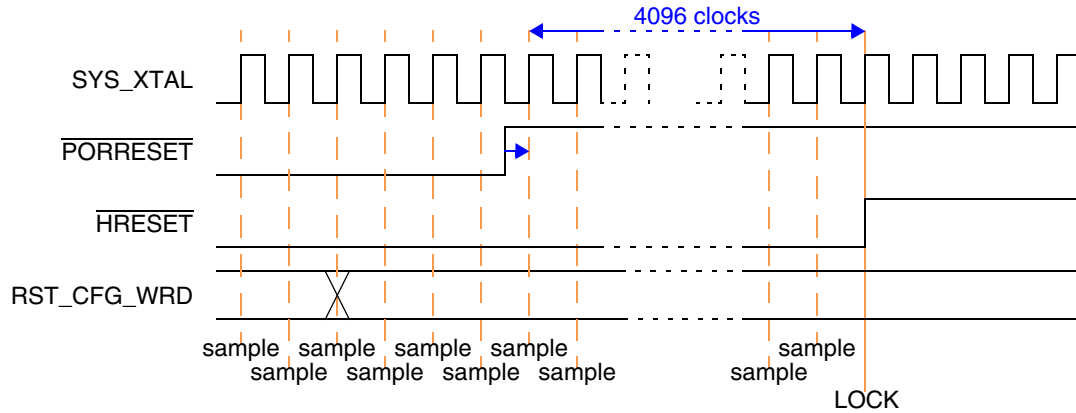


Figure 3. Reset Configuration Word Locking

NOTE

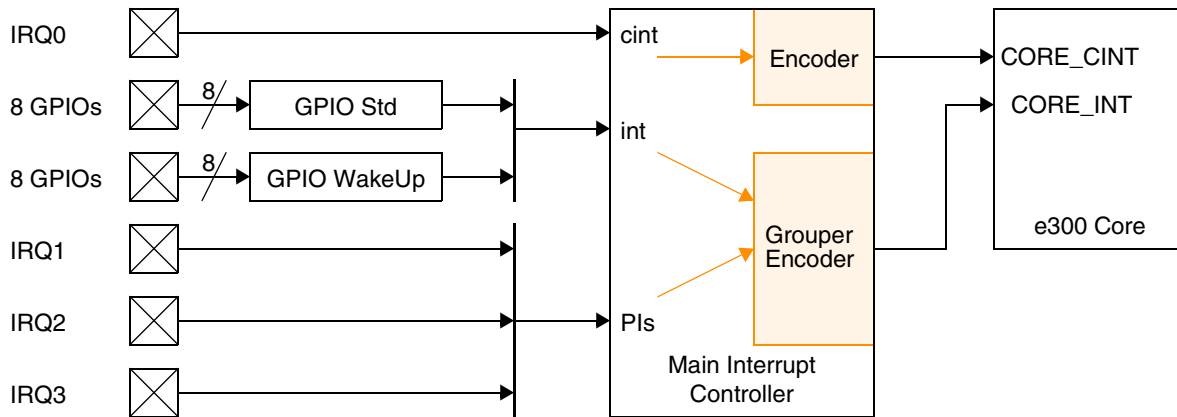
Beware of changing the values on the pins of the reset configuration word after the deassertion of $\overline{\text{PORRESET}}$. This may cause problems because it may change the internal clock ratios and so extend the PLL locking process.

1.3.5 External Interrupts

The MPC5200B provides three different kinds of external interrupts:

- Four IRQ interrupts
- Eight GPIO interrupts with simple interrupt capability (not available in power-down mode)
- Eight WakeUp interrupts (special GPIO pins)

The propagation of these three kinds of interrupts to the core is shown in the following graphic:



- Notes:**
1. Pis = Programmable Inputs
 2. Grouper and Encoder functions imply programmability in software

Figure 4. External Interrupt Scheme

Due to synchronization, prioritization, and mapping of external interrupt sources, the propagation of external interrupts to the core processor is delayed by several IP_CLK clock cycles. The following table specifies the interrupt latencies in IP_CLK cycles. The IP_CLK frequency is programmable in the Clock Distribution Module (see Table 16).

Table 16. External Interrupt Latencies

| Interrupt Type | Pin Name | Clock Cycles | Reference Clock | Core Interrupt | SpecID |
|--------------------------|-------------|--------------|-----------------|-----------------|--------|
| Interrupt Requests | IRQ0 | 10 | IP_CLK | critical (cint) | A4.1 |
| | IRQ0 | 10 | IP_CLK | normal (int) | A4.2 |
| | IRQ1 | 10 | IP_CLK | normal (int) | A4.3 |
| | IRQ2 | 10 | IP_CLK | normal (int) | A4.4 |
| | IRQ3 | 10 | IP_CLK | normal (int) | A4.5 |
| Standard GPIO Interrupts | GPIO_PSC3_4 | 12 | IP_CLK | normal (int) | A4.6 |
| | GPIO_PSC3_5 | 12 | IP_CLK | normal (int) | A4.7 |
| | GPIO_PSC3_8 | 12 | IP_CLK | normal (int) | A4.8 |
| | GPIO_USB_9 | 12 | IP_CLK | normal (int) | A4.9 |
| | GPIO_ETH1_4 | 12 | IP_CLK | normal (int) | A4.10 |
| | GPIO_ETH1_5 | 12 | IP_CLK | normal (int) | A4.11 |
| | GPIO_ETH1_6 | 12 | IP_CLK | normal (int) | A4.12 |
| | GPIO_ETH1_7 | 12 | IP_CLK | normal (int) | A4.13 |
| GPIO WakeUp Interrupts | GPIO_PSC1_4 | 12 | IP_CLK | normal (int) | A4.15 |
| | GPIO_PSC2_4 | 12 | IP_CLK | normal (int) | A4.16 |
| | GPIO_PSC3_9 | 12 | IP_CLK | normal (int) | A4.17 |
| | GPIO_ETH1_8 | 12 | IP_CLK | normal (int) | A4.18 |
| | GPIO_IRDA_0 | 12 | IP_CLK | normal (int) | A4.19 |
| | DGP_IN0 | 12 | IP_CLK | normal (int) | A4.20 |
| | DGP_IN1 | 12 | IP_CLK | normal (int) | A4.21 |

NOTES:

- 1) The frequency of IP_CLK depends on register settings in Clock Distribution Module. See the MPC5200B User Manual.

2) The interrupt latency descriptions in the table above are related to non competitive, non masked but enabled external interrupt sources. Take care of interrupt prioritization which may increase the latencies.

Because all external interrupt signals are synchronized into the internal processor bus clock domain, each of these signals has to exceed a minimum pulse width of more than one IP_CLK cycle.

Table 17. Minimum Pulse Width for External Interrupts to be Recognized

| Name | Min Pulse Width | Max Pulse Width | Reference Clock | SpecID |
|---------------------------------------|-----------------|-----------------|-----------------|--------|
| All external interrupts (IRQs, GPIOs) | > 1 clock cycle | — | IP_CLK | A4.22 |

NOTES:

- 1) The frequency of the IP_CLK depends on the register settings in Clock Distribution Module. See the MPC5200B User Manual for further information.
- 2) If the same interrupt occurs a second time while its interrupt service routine has not cleared the former one, the second interrupt is not recognized at all.

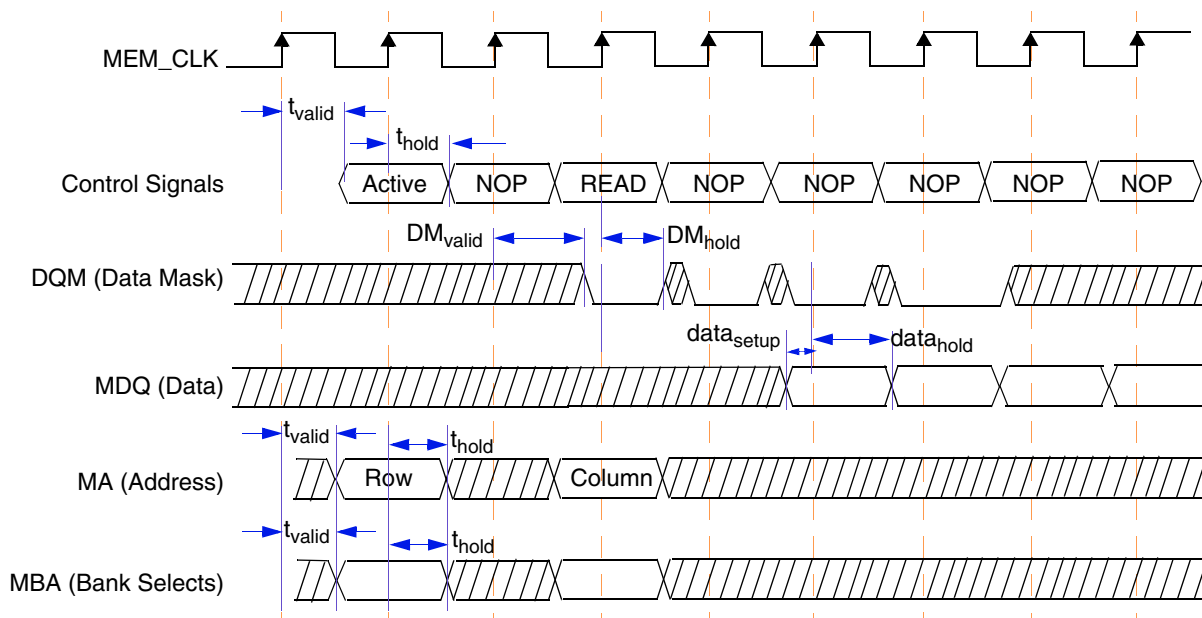
Besides synchronization, prioritization, and mapping the latency of an external interrupt to the start of its associated interrupt service routine also depends on the following conditions: To get a minimum interrupt service response time, it is recommended to enable the instruction cache and set up the maximum core clock, XL bus, and IP bus frequencies (depending on board design and programming). In addition, it is advisable to execute an interrupt handler, which has been implemented in assembly code.

1.3.6 SDRAM

1.3.6.1 Memory Interface Timing-Standard SDRAM Read Command

Table 18. Standard SDRAM Memory Read Timing

| Sym | Description | Min | Max | Units | SpecID |
|----------------|---|-----------------------------|-----------------------------|-------|--------|
| t_{mem_clk} | MEM_CLK period | 7.5 | — | ns | A5.1 |
| t_{valid} | Control Signals, Address and MBA Valid after rising edge of MEM_CLK | — | $t_{mem_clk} * 0.5 + 0.4$ | ns | A5.2 |
| t_{hold} | Control Signals, Address and MBA Hold after rising edge of MEM_CLK | $t_{mem_clk} * 0.5$ | — | ns | A5.3 |
| DM_{valid} | DQM valid after rising edge of MEM_CLK | — | $t_{mem_clk} * 0.25 + 0.4$ | ns | A5.4 |
| DM_{hold} | DQM hold after rising edge of MEM_CLK | $t_{mem_clk} * 0.25 - 0.7$ | — | ns | A5.5 |
| $data_{setup}$ | MDQ setup to rising edge of MEM_CLK | — | 0.3 | ns | A5.6 |
| $data_{hold}$ | MDQ hold after rising edge of MEM_CLK | 0.2 | — | ns | A5.7 |



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM_WE}}$, $\overline{\text{MEM_CS}}$, $\overline{\text{MEM_CS1}}$ and CLK_EN

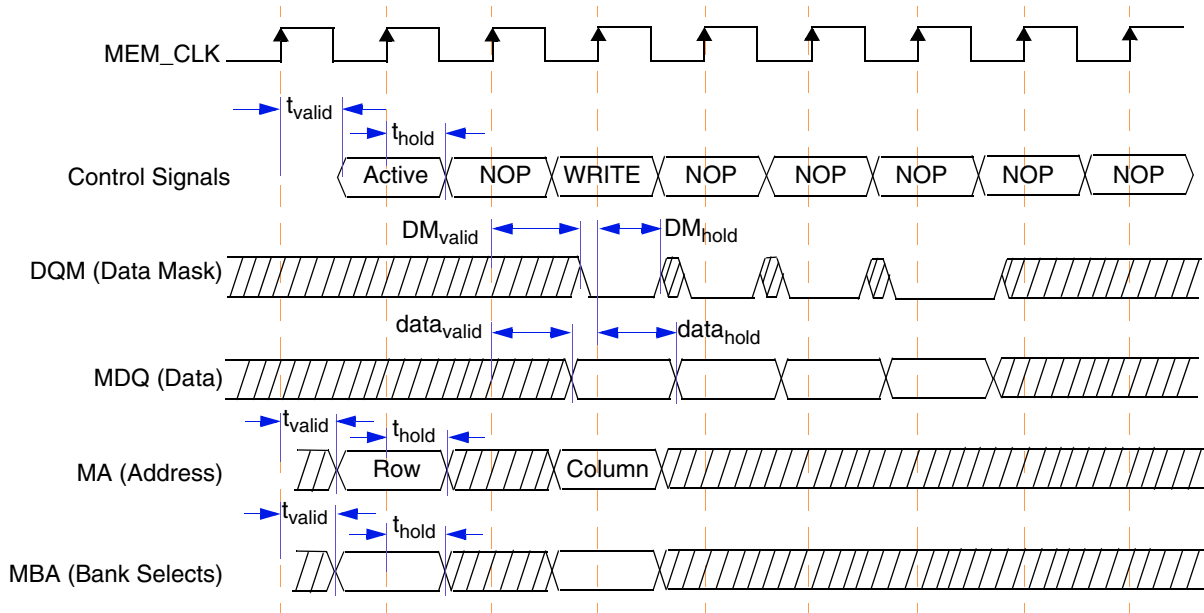
Figure 5. Timing Diagram—Standard SDRAM Memory Read Timing

1.3.6.2 Memory Interface Timing-Standard SDRAM Write Command

In Standard SDRAM, all signals are activated on the MEM_CLK from the Memory Controller and captured on the MEM_CLK clock at the memory device.

Table 19. Standard SDRAM Write Timing

| Sym | Description | Min | Max | Units | SpecID |
|------------------------------|---|------------------------------------|------------------------------------|-------|--------|
| $t_{\text{mem_clk}}$ | MEM_CLK period | 7.5 | — | ns | A5.8 |
| t_{valid} | Control Signals, Address and MBA Valid after rising edge of MEM_CLK | — | $t_{\text{mem_clk}} * 0.5 + 0.4$ | ns | A5.9 |
| t_{hold} | Control Signals, Address and MBA Hold after rising edge of MEM_CLK | $t_{\text{mem_clk}} * 0.5$ | — | ns | A5.10 |
| DM_{valid} | DQM valid after rising edge of MEM_CLK | — | $t_{\text{mem_clk}} * 0.25 + 0.4$ | ns | A5.11 |
| DM_{hold} | DQM hold after rising edge of Mem_clk | $t_{\text{mem_clk}} * 0.25 - 0.7$ | — | ns | A5.12 |
| $\text{data}_{\text{valid}}$ | MDQ valid after rising edge of MEM_CLK | — | $t_{\text{mem_clk}} * 0.75 + 0.4$ | ns | A5.13 |
| $\text{data}_{\text{hold}}$ | MDQ hold after rising edge of MEM_CLK | $t_{\text{mem_clk}} * 0.75 - 0.7$ | — | ns | A5.14 |



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM_WE}}$, $\overline{\text{MEM_CS}}$, $\overline{\text{MEM_CS1}}$ and CLK_EN

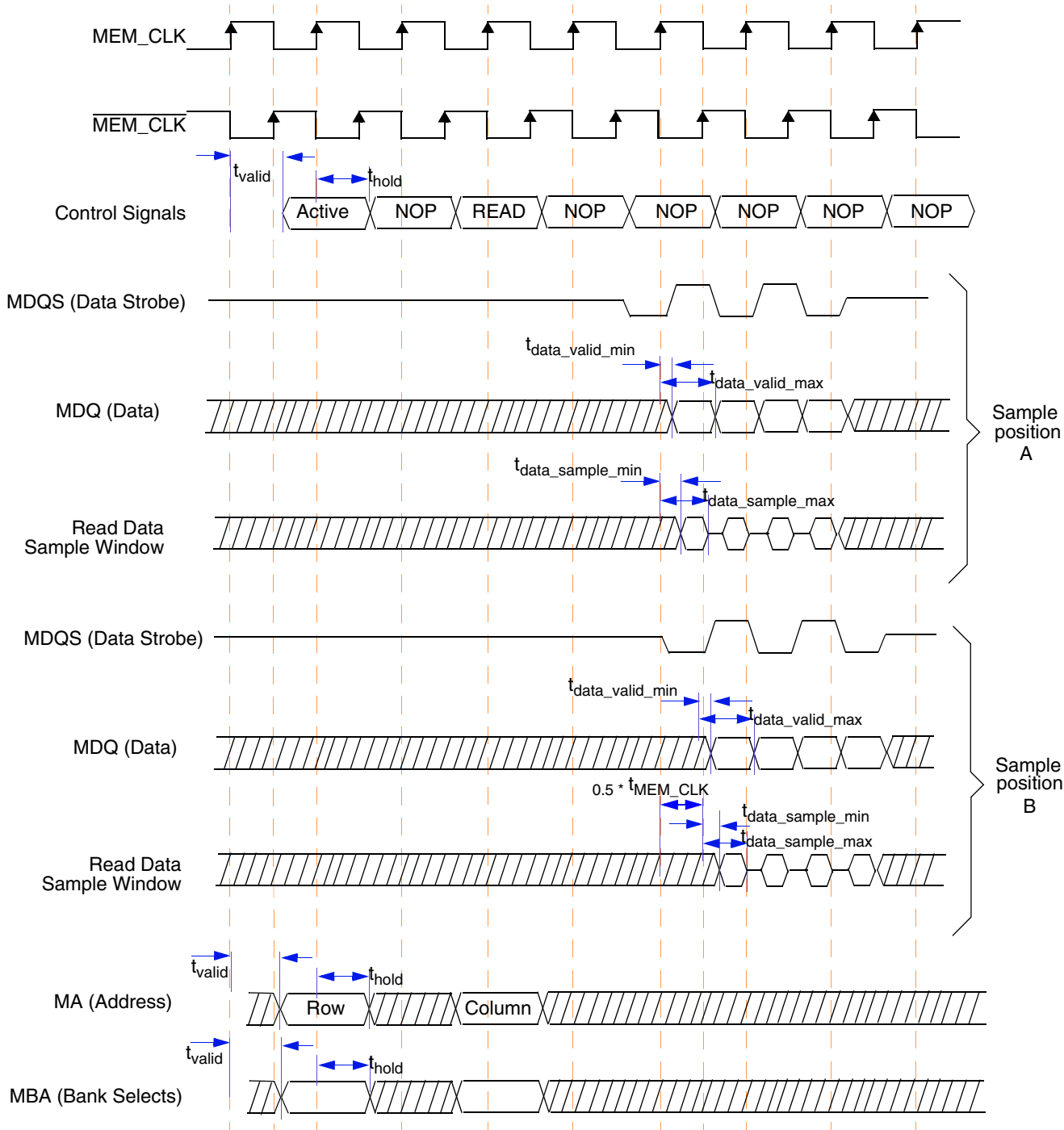
Figure 6. Timing Diagram—Standard SDRAM Memory Write Timing

1.3.6.3 Memory Interface Timing-DDR SDRAM Read Command

The SDRAM Memory Controller uses a 1/4 period delayed MDQS strobe to capture the MDQ data. The 1/4 period delay value is calculated automatically by hardware.

Table 20. DDR SDRAM Memory Read Timing

| Sym | Description | Min | Max | Units | SpecID |
|------------------------------|---|-----------------------------|-----------------------------------|-------|--------|
| $t_{\text{mem_clk}}$ | MEM_CLK period | 7.5 | — | ns | A5.15 |
| t_{valid} | Control Signals, Address and MBA valid after rising edge of MEM_CLK | — | $t_{\text{mem_clk}} * 0.5 + 0.4$ | ns | A5.16 |
| t_{hold} | Control Signals, Address and MBA hold after rising edge of MEM_CLK | $t_{\text{mem_clk}} * 0.5$ | — | ns | A5.17 |
| $\text{data}_{\text{setup}}$ | Setup time relative to MDQS | — | 0.4 | ns | A5.18 |
| $\text{data}_{\text{hold}}$ | Hold time relative to MDQS | 2.6 | — | ns | A5.19 |



Sample position A: data are sampled on the expected edge of MEM_CLK, the MDQS signal indicate the valid data
 Sample position B: data are sampled on a later edge of MEM_CLK, SDRAM controller is waiting for the valid MDQS signal

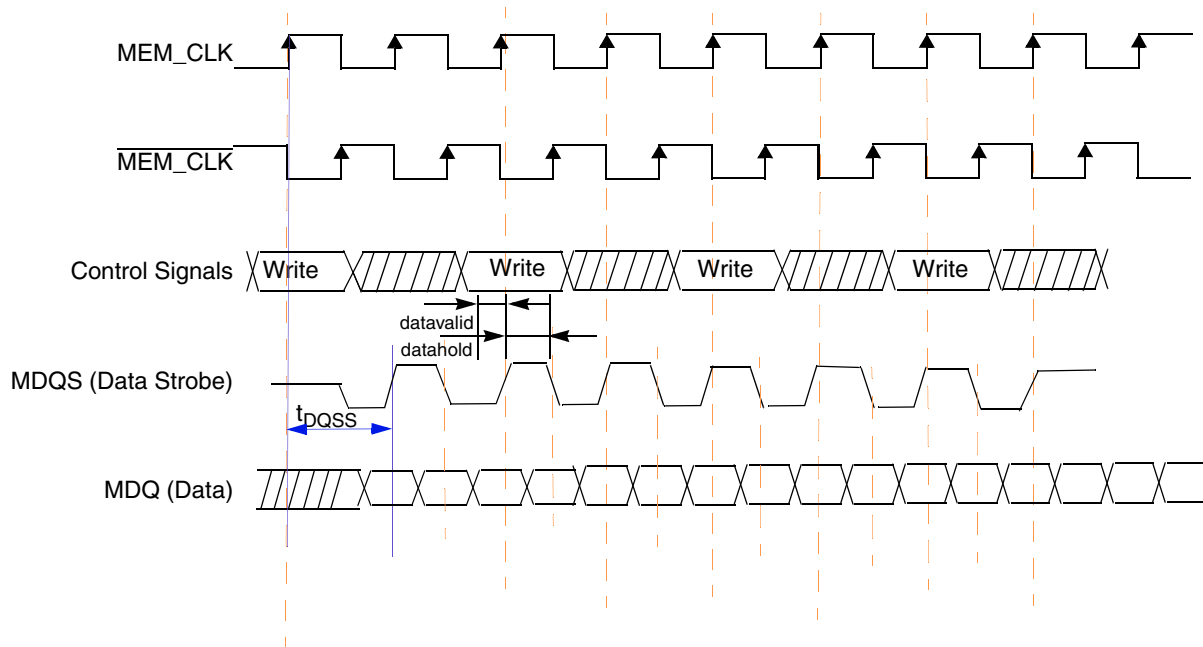
NOTE: Control Signals signals are composed of RAS, CAS, $\overline{MEM_WE}$, $\overline{MEM_CS}$, $\overline{MEM_CS1}$ and CLK_EN

Figure 7. Timing Diagram—DDR SDRAM Memory Read Timing

1.3.6.4 Memory Interface Timing-DDR SDRAM Write Command

Table 21. DDR SDRAM Memory Write Timing

| Sym | Description | Min | Max | Units | SpecID |
|----------------|---|-----|--------------------|-------|--------|
| t_{mem_clk} | MEM_CLK period | 7.5 | — | ns | A5.20 |
| t_{DQSS} | Delay from write command to first rising edge of MDQS | — | $t_{mem_clk}+0.4$ | ns | A5.21 |
| $data_{valid}$ | MDQ valid before rising edge of MDQS | 1.0 | — | ns | A5.22 |
| $data_{hold}$ | MDQ valid after rising edge of MDQS | 1.0 | — | ns | A5.23 |



NOTE: Control Signals signals are composed of RAS, CAS, $\overline{MEM_WE}$, $\overline{MEM_CS}$, $\overline{MEM_CS1}$, and CLK_EN

Figure 8. DDR SDRAM Memory Write Timing

1.3.7 PCI

The PCI interface on the MPC5200B is designed to PCI Version 2.2 and supports 33-MHz and 66-MHz PCI operations. See the PCI Local Bus Specification; the component section specifies the electrical and timing parameters for PCI components with the intent that components connect directly together whether on the planar or an expansion board, without any external buffers or other “glue logic.” Parameters apply at the package pins, not at expansion board edge connectors.

The MPC5200B is always the source of the PCI CLK. The clock waveform must be delivered to each 33-MHz or 66-MHz PCI component in the system. Figure 9 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 22 summarizes the clock specifications.

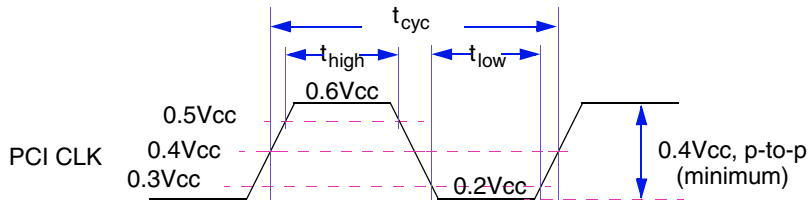


Figure 9. PCI CLK Waveform

Table 22. PCI CLK Specifications

| Sym | Description | 66 MHz | | 33 MHz | | Units | Notes | SpecID |
|------------|---------------------------------|--------|-----|--------|-----|-------|---------|--------|
| | | Min | Max | Min | Max | | | |
| t_{cyc} | PCI CLK Cycle Time | 15 | 30 | 30 | | ns | (1),(3) | A6.1 |
| t_{high} | PCI CLK High Time | 6 | | 11 | | ns | | A6.2 |
| t_{low} | PCI CLK Low Time | 6 | | 11 | | ns | | A6.3 |
| — | PCI CLK Slew Rate | 1.5 | 4 | 1 | 4 | V/ns | (2) | A6.4 |
| — | PCI Clock Jitter (peak to peak) | | 200 | | 200 | ps | | |

NOTES:

1. In general, all 66-MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 9.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

Table 23. PCI Timing Parameters

| Sym | Description | 66 MHz | | 33 MHz | | Units | Notes | SpecID |
|----------------|--|--------|-----|--------|-----|-------|-------------|--------|
| | | Min | Max | Min | Max | | | |
| t_{val} | CLK to Signal Valid Delay - bused signals | 2 | 6 | 2 | 11 | ns | (1),(2),(3) | A6.5 |
| $t_{val}(ptp)$ | CLK to Signal Valid Delay - point to point | 2 | 6 | 2 | 12 | ns | (1),(2),(3) | A6.6 |
| t_{on} | Float to Active Delay | 2 | | 2 | | ns | (1) | A6.7 |
| t_{off} | Active to Float Delay | | 14 | | 28 | ns | (1) | A6.8 |
| t_{su} | Input Setup Time to CLK - bused signals | 3 | | 7 | | ns | (3),(4) | A6.9 |
| $t_{su}(ptp)$ | Input Setup Time to CLK - point to point | 5 | | 10,12 | | ns | (3),(4) | A6.10 |
| t_h | Input Hold Time from CLK | 0 | | 0 | | ns | (4) | A6.11 |

NOTES:

1. See the timing measurement conditions in the PCI Local Bus Specification. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.

2. Minimum times are measured at the package pin with the load circuit, and maximum times are measured with the load circuit as shown in the PCI Local Bus Specification.
3. REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.
4. See the timing measurement conditions in the PCI Local Bus Specification.

For Measurement and Test Conditions, see the PCI Local Bus Specification.

1.3.8 Local Plus Bus

The Local Plus Bus is the external bus interface of the MPC5200B. A maximum of eight configurable chip selects (CS) are provided. There are two main modes of operation: non-MUXed (Legacy and Burst) and MUXED. The reference clock is the PCI CLK. The maximum bus frequency is 66 MHz.

Definition of Acronyms and Terms:

- WS = Wait State
- DC = Dead Cycle
- LB = Long Burst
- DS = Data Size in Bytes
- t_{PClk} = PCI clock period
- t_{IPBck} = IPBI clock period

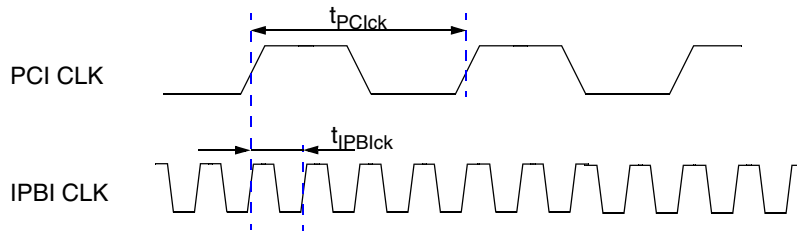


Figure 10. Timing Diagram—IPBI and PCI clock (example ratio: 4:1)

1.3.8.1 Non-MUXed Mode

Table 24. Non-MUXed Mode Timing

| Sym | Description | Min | Max | Units | Notes | SpecID |
|-----------|---------------------------------------|-------------------|-------------------|-------|-------|--------|
| t_{CSA} | PCI CLK to CS assertion | 4.6 | 10.6 | ns | | A7.1 |
| t_{CSN} | PCI CLK to CS negation | 2.9 | 7.0 | ns | | A7.2 |
| t_1 | CS pulse width | $(2+WS)*t_{PClk}$ | $(2+WS)*t_{PClk}$ | ns | (1) | A7.3 |
| t_2 | ADDR valid before CS assertion | t_{IPBck} | t_{PClk} | ns | | A7.4 |
| t_3 | ADDR hold after CS negation | t_{IPBck} | - | ns | (2) | A7.5 |
| t_4 | OE assertion before CS assertion | - | 4.8 | ns | | A7.6 |
| t_5 | OE negation before CS negation | - | 2.7 | ns | | A7.7 |
| t_6 | RW valid before CS assertion | t_{PClk} | - | ns | | A7.8 |
| t_7 | RW hold after CS negation | t_{IPBck} | - | ns | | A7.9 |
| t_8 | DATA output valid before CS assertion | t_{IPBck} | - | ns | | A7.10 |
| t_9 | DATA output hold after CS negation | t_{IPBck} | - | ns | | A7.11 |

Table 24. Non-MUXed Mode Timing (continued)

| Sym | Description | Min | Max | Units | Notes | SpecID |
|-----------------|-------------------------------------|----------------------|---------------------------|-------|-------|--------|
| t ₁₀ | DATA input setup before CS negation | 8.5 | - | ns | | A7.12 |
| t ₁₁ | DATA input hold after CS negation | 0 | (DC+1)*t _{PClck} | ns | (6) | A7.13 |
| t ₁₂ | ACK assertion after CS assertion | t _{PClck} | - | ns | (3) | A7.14 |
| t ₁₃ | ACK negation after CS negation | - | t _{PClck} | ns | (3) | A7.15 |
| t ₁₄ | TS assertion before CS assertion | - | 6.9 | ns | (4) | A7.16 |
| t ₁₅ | TS pulse width | t _{PClck} | t _{PClck} | ns | (4) | A7.17 |
| t ₁₆ | TSIZ valid before CS assertion | t _{IPBclck} | - | ns | (5) | A7.18 |
| t ₁₇ | TSIZ hold after CS negation | t _{IPBclck} | - | ns | (5) | A7.19 |
| t ₁₈ | ACK change before PCI clock | - | 2.0 | ns | (1) | A7.20 |
| t ₁₉ | ACK change after PCI clock | - | 4.4 | ns | (1) | A7.21 |

NOTES:

1. ACK can shorten the CS pulse width.
Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0 - 65535.
2. In Large Flash and MOST Graphics mode the shared PCI/ATA pins, used as address lines, are released at the same moment as the CS. This can cause the address to change before CS is deasserted.
3. ACK is input and can be used to shorten the CS pulse width.
4. Only available in Large Flash and MOST Graphics mode.
5. Only available in MOST Graphics mode.
6. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

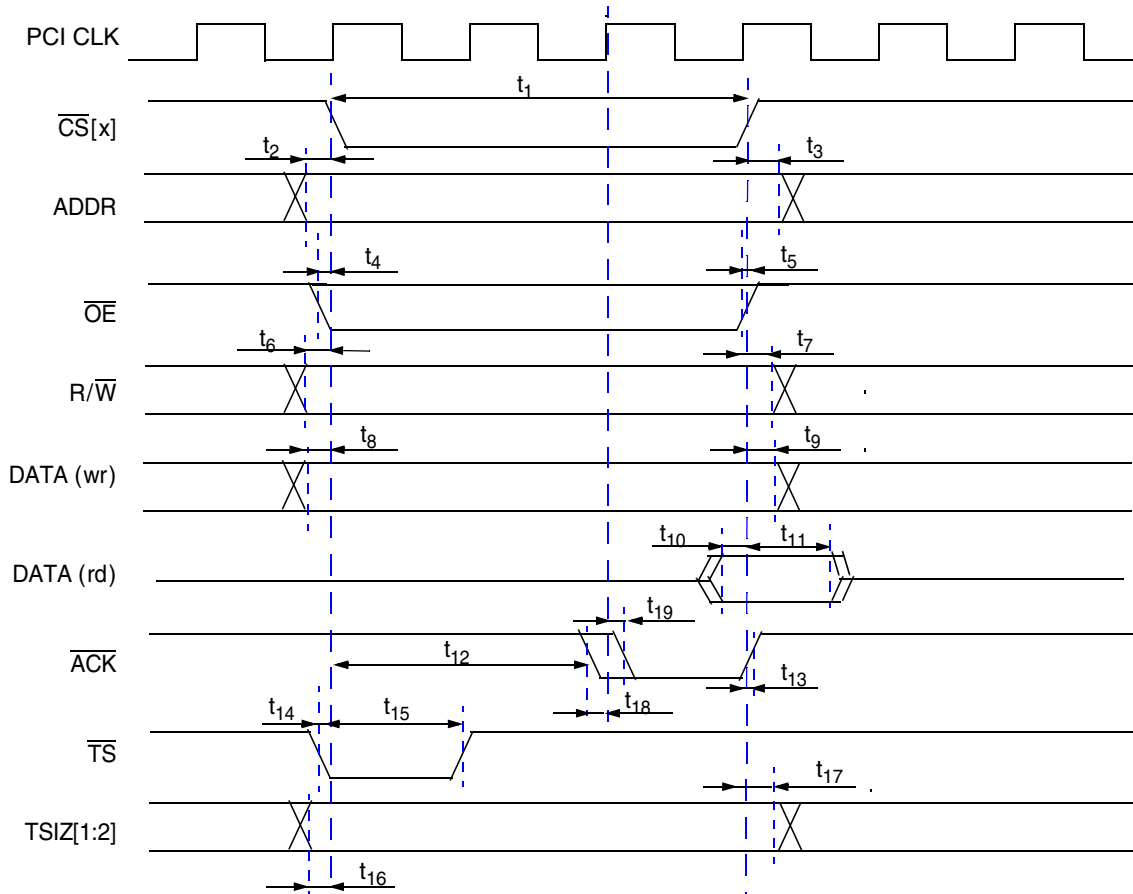


Figure 11. Timing Diagram—Non-MUXed Mode

1.3.8.2 Burst Mode

Table 25. Burst Mode Timing

| Sym | Description | Min | Max | Units | Notes | SpecID |
|------------------|--|--------------------------------------|--------------------------------------|-------|---------|--------|
| t _{CSA} | PCI CLK to CS assertion | 4.6 | 10.6 | ns | | A7.22 |
| t _{CSN} | PCI CLK to CS negation | 2.9 | 7.0 | ns | | A7.23 |
| t ₁ | CS pulse width | $(1+WS+4^{LB*2}*(32/DS))^* t_{PCLK}$ | $(1+WS+4^{LB*2}*(32/DS)) * t_{PCLK}$ | ns | (1),(2) | A7.24 |
| t ₂ | ADDR valid before CS assertion | t _{IPBclk} | t _{PCLK} | ns | | A7.25 |
| t ₃ | ADDR hold after CS negation | -0.7 | - | ns | | A7.26 |
| t ₄ | OE assertion before CS assertion | - | 4.8 | ns | | A7.27 |
| t ₅ | OE negation before CS negation | - | 2.7 | ns | | A7.28 |
| t ₆ | RW valid before CS assertion | t _{PCLK} | - | ns | | A7.29 |
| t ₇ | RW hold after CS negation | t _{PCLK} | - | ns | | A7.30 |
| t ₈ | DATA setup before rising edge of PCI clock | 3.6 | - | ns | | A7.31 |

Table 25. Burst Mode Timing (continued)

| Sym | Description | Min | Max | Units | Notes | SpecID |
|-----------------|--|--|--|-------|---------|--------|
| t ₉ | DATA hold after rising edge of PCI clock | 0 | - | ns | | A7.32 |
| t ₁₀ | DATA hold after CS negation | 0 | (DC+1)*t _{PClk} | ns | (4) | A7.33 |
| t ₁₁ | ACK assertion after CS assertion | - | (WS+1)*t _{PClk} | ns | | A7.34 |
| t ₁₂ | ACK negation before CS negation | - | 7.0 | ns | (3) | A7.35 |
| t ₁₃ | ACK pulse width | 4 ^{LB} *2*(32/DS)*t _{PClk} | 4 ^{LB} *2*(32/DS)*t _{PClk} | ns | (2),(3) | A7.36 |
| t ₁₄ | CS assertion after TS assertion | - | 2.5 | ns | | A7.37 |
| t ₁₅ | TS pulse width | t _{PClk} | t _{PClk} | ns | | A7.38 |

NOTES:

- Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0 - 65535.
- Example:
 Long Burst is used, this means the CS related BERx and SLB bits of the Chip Select Burst Control Register are set and a burst on the internal XLB is executed. => LB = 1
 Data bus width is 8 bit. => DS = 8
 => 4¹*2*(32/8) = 32 => ACK is asserted for 32 PCI cycles to transfer one cache line.
 Wait State is set to 10. => WS = 10
 1+10+32 = 43 => CS is asserted for 43 PCI cycles.
- ACK is output and indicates the burst.
- Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

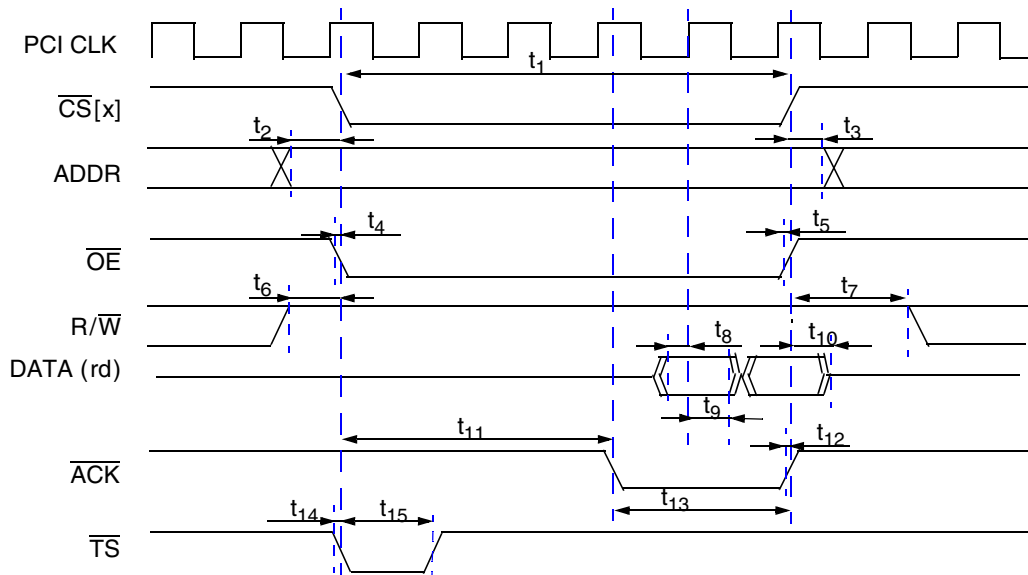


Figure 12. Timing Diagram—Burst Mode

1.3.8.3 MUXed Mode

Table 26. MUXed Mode Timing

| Sym | Description | Min | Max | Units | Notes | SpecID |
|-------------------|--|--------------------------|--------------------------|-------|---------|--------|
| t _{CSA} | PCI CLK to CS assertion | 4.6 | 10.6 | ns | | A7.39 |
| t _{CSN} | PCI CLK to CS negation | 2.9 | 7.0 | ns | | A7.40 |
| t _{ALEA} | PCI CLK to ALE assertion | - | 3.6 | ns | | A7.41 |
| t ₁ | ALE assertion before Address, Bank, TSIZ assertion | - | 5.7 | ns | | A7.42 |
| t ₂ | CS assertion before Address, Bank, TSIZ negation | - | -1.2 | ns | | A7.43 |
| t ₃ | CS assertion before Data wr valid | - | -1.2 | ns | | A7.44 |
| t ₄ | Data wr hold after CS negation | t _{IPBclk} | - | ns | | A7.45 |
| t ₅ | Data rd setup before CS negation | 8.5 | - | ns | | A7.46 |
| t ₆ | Data rd hold after CS negation | 0 | (DC+1)*t _{PClk} | ns | (1),(3) | A7.47 |
| t ₇ | ALE pulse width | - | t _{PClk} | ns | | A7.48 |
| t _{TSA} | CS assertion after TS assertion | - | 6.9 | ns | | A7.49 |
| t ₈ | TS pulse width | - | t _{PClk} | ns | | A7.50 |
| t ₉ | CS pulse width | (2+WS)*t _{PClk} | (2+WS)*t _{PClk} | ns | | A7.51 |
| t _{OEA} | OE assertion before CS assertion | - | 4.7 | ns | | A7.52 |
| t _{OEN} | OE negation before CS negation | - | 5.9 | ns | | A7.53 |
| t ₁₀ | RW assertion before ALE assertion | t _{IPBclk} | - | ns | | A7.54 |
| t ₁₁ | RW negation after CS negation | - | t _{PClk} | ns | | A7.55 |
| t ₁₂ | ACK assertion after CS assertion | t _{IPBclk} | - | ns | (2) | A7.56 |
| t ₁₃ | ACK negation after CS negation | - | t _{PClk} | ns | (2) | A7.57 |
| t ₁₄ | ALE negation to CS assertion | - | t _{PClk} | ns | | A7.58 |
| t ₁₅ | ACK change before PCI clock | - | 2.0 | ns | (2) | A7.59 |
| t ₁₆ | ACK change after PCI clock | - | 4.4 | ns | (2) | A7.60 |

NOTES:

1. ACK can shorten the CS pulse width.
Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0 - 65535.
2. ACK is input and can be used to shorten the CS pulse width.
3. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

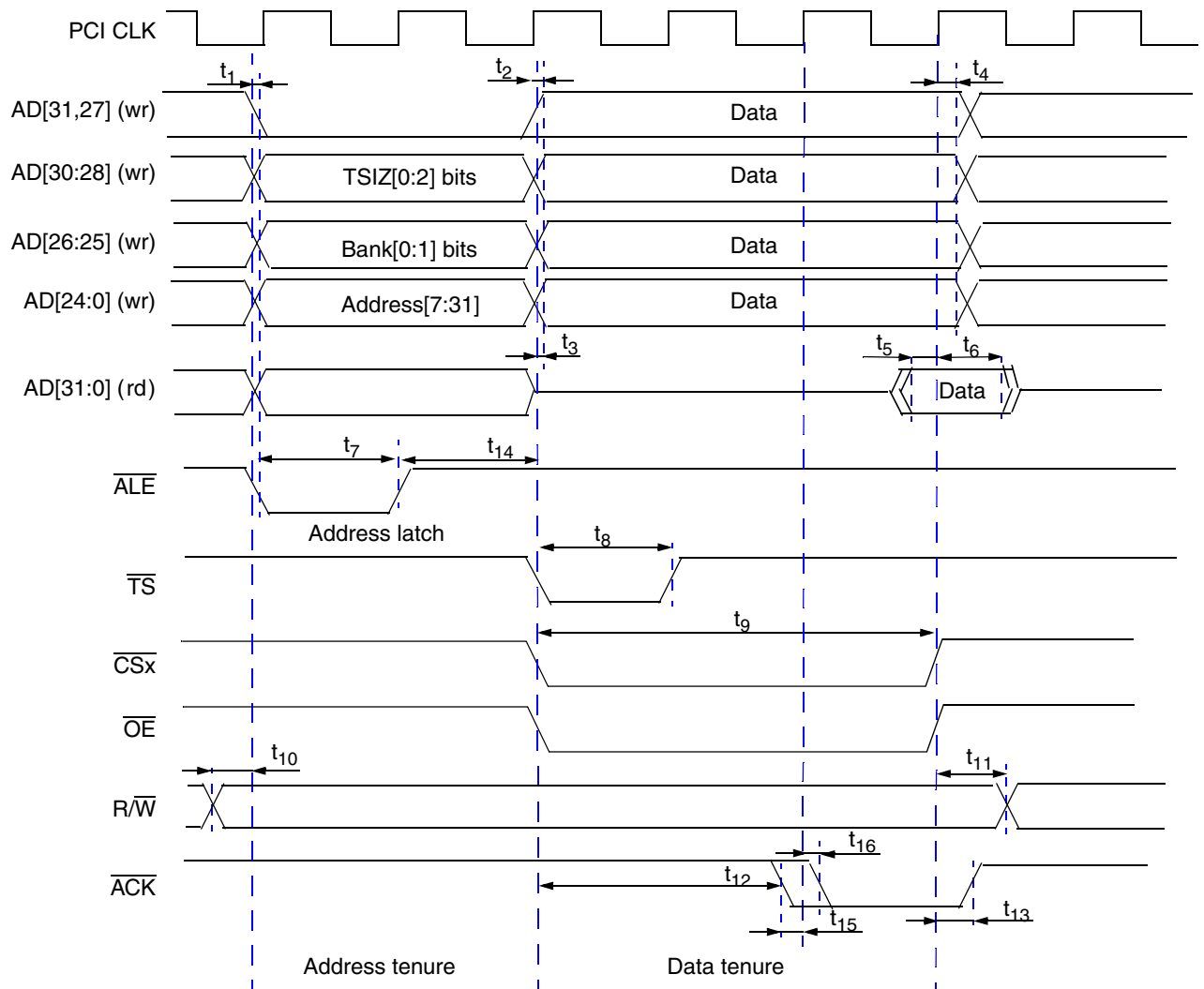


Figure 13. Timing Diagram—MUXed Mode

1.3.9 ATA

The MPC5200B ATA Controller is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nanoseconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the MPC5200B User Manual.

The MPC5200B ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup-time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold-time beyond that required by the ATA-4 specification.

All ATA transfers are programmed in terms of system clock cycles (IP bus clocks) in the ATA Host Controller timing registers. This puts constraints on the ATA protocols and their respective timing modes in which the ATA Controller can communicate with the drive.

Faster ATA modes (i.e., UDMA 0, 1, 2) are supported when the system is running at a sufficient frequency to provide adequate data transfer rates. Adequate data transfer rates are a function of the following:

- The MPC5200B operating frequency (IP bus clock frequency)
- Internal MPC5200B bus latencies
- Other system load dependent variables

The ATA clock is the same frequency as the IP bus clock in MPC5200B. See the MPC5200B User Manual.

NOTE

All output timing numbers are specified for nominal 50 pF loads.

Table 27. PIO Mode Timing Specifications

| Sym | PIO Timing Parameter | Min/Max (ns) | Mode 0 (ns) | Mode 1 (ns) | Mode 2 (ns) | Mode 3 (ns) | Mode 4 (ns) | SpecID |
|-----------------|---|--------------|-------------|-------------|-------------|-------------|-------------|--------|
| t ₀ | Cycle Time | min | 600 | 383 | 240 | 180 | 120 | A8.1 |
| t ₁ | Address valid to $\overline{\text{DIOR}}/\overline{\text{DIOW}}$ setup | min | 70 | 50 | 30 | 30 | 25 | A8.2 |
| t ₂ | $\overline{\text{DIOR}}/\overline{\text{DIOW}}$ pulse width 16-bit 8-bit | min min | 165 290 | 125 290 | 100 290 | 80 80 | 70 70 | A8.3 |
| t _{2i} | $\overline{\text{DIOR}}/\overline{\text{DIOW}}$ recovery time | min | — | — | — | 70 | 25 | A8.4 |
| t ₃ | $\overline{\text{DIOW}}$ data setup | min | 60 | 45 | 30 | 30 | 20 | A8.5 |
| t ₄ | $\overline{\text{DIOW}}$ data hold | min | 30 | 20 | 15 | 10 | 10 | A8.6 |
| t ₅ | $\overline{\text{DIOR}}$ data setup | min | 50 | 35 | 20 | 20 | 20 | A8.7 |
| t ₆ | $\overline{\text{DIOR}}$ data hold | min | 5 | 5 | 5 | 5 | 5 | A8.8 |
| t ₉ | $\overline{\text{DIOR}}/\overline{\text{DIOW}}$ to address valid hold | min | 20 | 15 | 10 | 10 | 10 | A8.9 |
| t _A | IORDY setup | max | 35 | 35 | 35 | 35 | 35 | A8.10 |
| t _B | IORDY pulse width | max | 1250 | 1250 | 1250 | 1250 | 1250 | A8.11 |

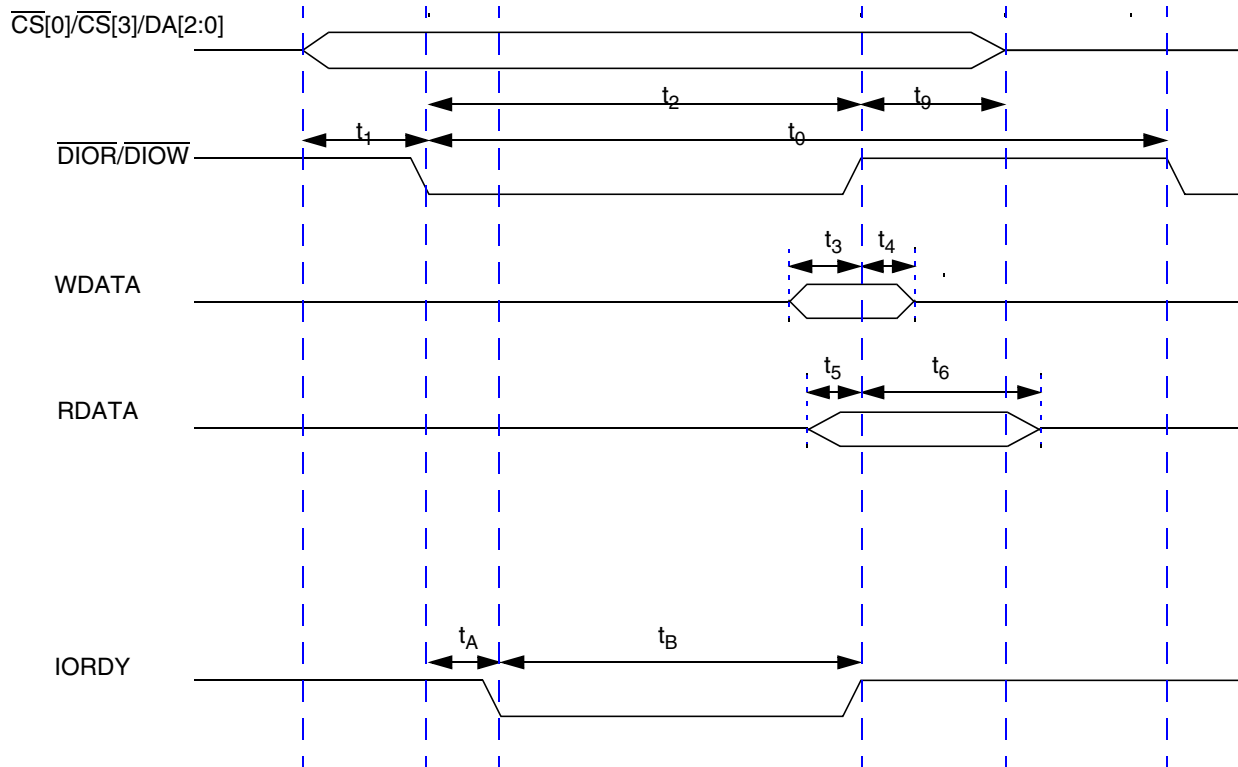


Figure 14. PIO Mode Timing

Table 28. Multiword DMA Timing Specifications

| Sym | Multiword DMA Timing Parameters | Min/Max | Mode 0(ns) | Mode 1(ns) | Mode 2(ns) | SpecID |
|----------|---|---------|------------|------------|------------|--------|
| t_0 | Cycle Time | min | 480 | 150 | 120 | A8.12 |
| t_C | \overline{DMACK} to \overline{DMARQ} delay | max | — | — | — | A8.13 |
| t_D | $\overline{DIOR}/\overline{DIOW}$ pulse width (16-bit) | min | 215 | 80 | 70 | A8.14 |
| t_E | \overline{DIOR} data access | max | 150 | 60 | 50 | A8.15 |
| t_G | $\overline{DIOR}/\overline{DIOW}$ data setup | min | 100 | 30 | 20 | A8.16 |
| t_F | \overline{DIOR} data hold | min | 5 | 5 | 5 | A8.17 |
| t_H | \overline{DIOW} data hold | min | 20 | 15 | 10 | A8.18 |
| t_I | \overline{DMACK} to $\overline{DIOR}/\overline{DIOW}$ setup | min | 0 | 0 | 0 | A8.19 |
| t_J | $\overline{DIOR}/\overline{DIOW}$ to \overline{DMACK} hold | min | 20 | 5 | 5 | A8.20 |
| t_{Kr} | \overline{DIOR} negated pulse width | min | 50 | 50 | 25 | A8.21 |
| t_{Kw} | \overline{DIOW} negated pulse width | min | 215 | 50 | 25 | A8.22 |
| t_{Lr} | \overline{DIOR} to \overline{DMARQ} delay | max | 120 | 40 | 35 | A8.23 |
| t_{Lw} | \overline{DIOW} to \overline{DMARQ} delay | max | 40 | 40 | 35 | A8.24 |

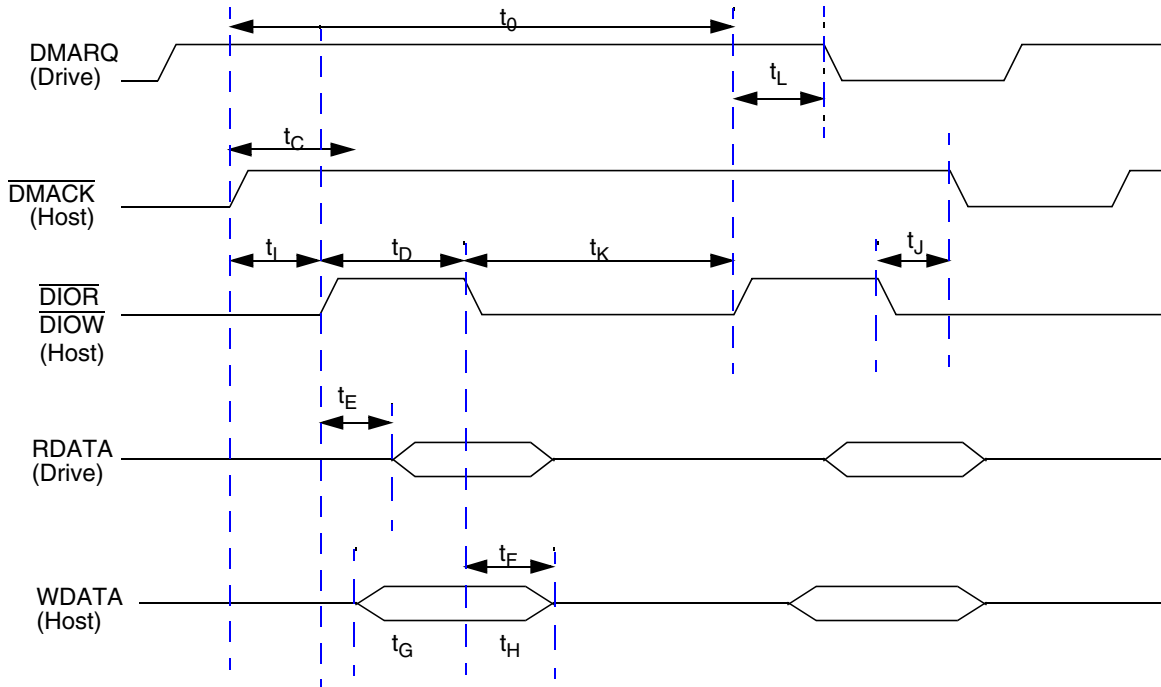


Figure 15. Multiword DMA Timing

NOTE

The direction of signal assertion is towards the top of the page, and the direction of negation is towards the bottom of the page, irrespective of the electrical properties of the signal.

Table 29. Ultra DMA Timing Specification

| Sym | MODE 0 (ns) | | MODE 1 (ns) | | MODE 2 (ns) | | Comment | SpecID |
|------------|-------------|-----|-------------|-----|-------------|-----|---|--------|
| | Min | Max | Min | Max | Min | Max | | |
| t_{CYC} | 114 | — | 75 | — | 55 | — | Cycle time allowing for asymmetry and clock variations from STROBE edge to STROBE edge | A8.26 |
| t_{2CYC} | 235 | — | 156 | — | 117 | — | Two-cycle time allowing for clock variations, from rising edge to next rising edge or from falling edge to next falling edge of STROBE. | A8.27 |
| t_{DS} | 15 | — | 10 | — | 7 | — | Data setup time at recipient. | A8.28 |
| t_{DH} | 5 | — | 5 | — | 5 | — | Data hold time at recipient. | A8.29 |
| t_{DVS} | 70 | — | 48 | — | 34 | — | Data valid setup time at sender, to STROBE edge. | A8.30 |
| t_{DVH} | 6 | — | 6 | — | 6 | — | Data valid hold time at sender, from STROBE edge. | A8.31 |
| t_{FS} | 0 | 230 | 0 | 200 | 0 | 170 | First STROBE time for drive to first negate DSTROBE from STOP during a data-in burst. | A8.32 |
| t_{LI} | 0 | 150 | 0 | 150 | 0 | 150 | Limited Interlock time. | A8.33 |
| t_{MLI} | 20 | — | 20 | — | 20 | — | Interlock time with minimum. | A8.34 |
| t_{UI} | 0 | — | 0 | — | 0 | — | Unlimited interlock time. | A8.35 |

Table 29. Ultra DMA Timing Specification (continued)

| Sym | MODE 0 (ns) | | MODE 1 (ns) | | MODE 2 (ns) | | Comment | SpecID |
|--------------|----------------|-----|----------------|-----|----------------|-----|---|--------|
| | Min | Max | Min | Max | Min | Max | | |
| t_{AZ} | — | 10 | — | 10 | — | 10 | Maximum time allowed for output drivers to release from being asserted or negated | A8.36 |
| t_{ZAH} | 20 | — | 20 | — | 20 | — | Minimum delay time required for output drivers to assert or negate from released state | A8.37 |
| t_{ZAD} | 0 | — | 0 | — | 0 | — | | A8.38 |
| t_{ENV} | 20 | 70 | 20 | 70 | 20 | 70 | Envelope time—from \overline{DMACK} to STOP and $\overline{HDMARDY}$ during data out burst initiation. | A8.39 |
| t_{SR} | — | 50 | — | 30 | — | 20 | STROBE to \overline{DMARDY} time, if \overline{DMARDY} is negated before this long after STROBE edge, the recipient receives no more than one additional data word. | A8.40 |
| t_{RFS} | — | 75 | — | 60 | — | 50 | Ready-to-Final STROBE time—no STROBE edges are sent this long after negation of \overline{DMARDY} . | A8.41 |
| t_{RP} | 160 | — | 125 | — | 100 | — | Ready-to-Pause time—the time recipient waits to initiate pause after negating \overline{DMARDY} . | A8.42 |
| t_{IORDYZ} | — | 20 | — | 20 | — | 20 | Pull-up time before allowing IORDY to be released. | A8.43 |
| t_{ZIORDY} | 0 | — | 0 | — | 0 | — | Minimum time drive waits before driving IORDY | A8.44 |
| t_{ACK} | 20 | — | 20 | — | 20 | — | Setup and hold times for \overline{DMACK} , before assertion or negation. | A8.45 |
| t_{SS} | 50 | — | 50 | — | 50 | — | Time from STROBE edge to negation of \overline{DMARQ} or assertion of STOP, when sender terminates a burst. | A8.46 |

NOTES:

- t_{UI} , t_{MLI} , t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks. That is, one agent (sender or recipient) is waiting for the other agent to respond with a signal before proceeding.
 - t_{UI} is an unlimited interlock that has no maximum time value.
 - t_{MLI} is a limited time-out that has a defined minimum.
 - t_{LI} is a limited time-out that has a defined maximum.
- All timing parameters are measured at the connector of the drive to which the parameter applies. For example, the sender shall stop generating STROBE edges t_{RFS} after negation of \overline{DMARDY} . STROBE and \overline{DMARDY} timing measurements are taken at the connector of the sender. Even though the sender stops generating STROBE edges, the receiver may receive additional STROBE edges due to propagation delays. All timing measurement switching points (low to high and high to low) are taken at 1.5 V.

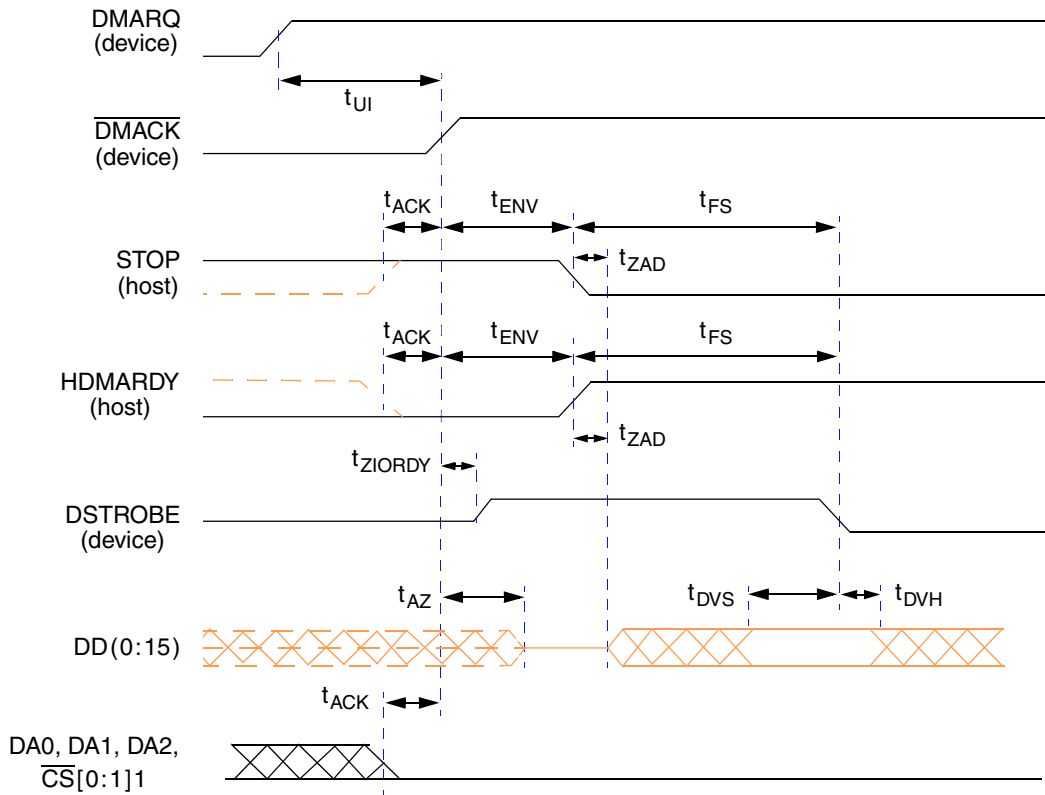


Figure 16. Timing Diagram—Initiating an Ultra DMA Data In Burst

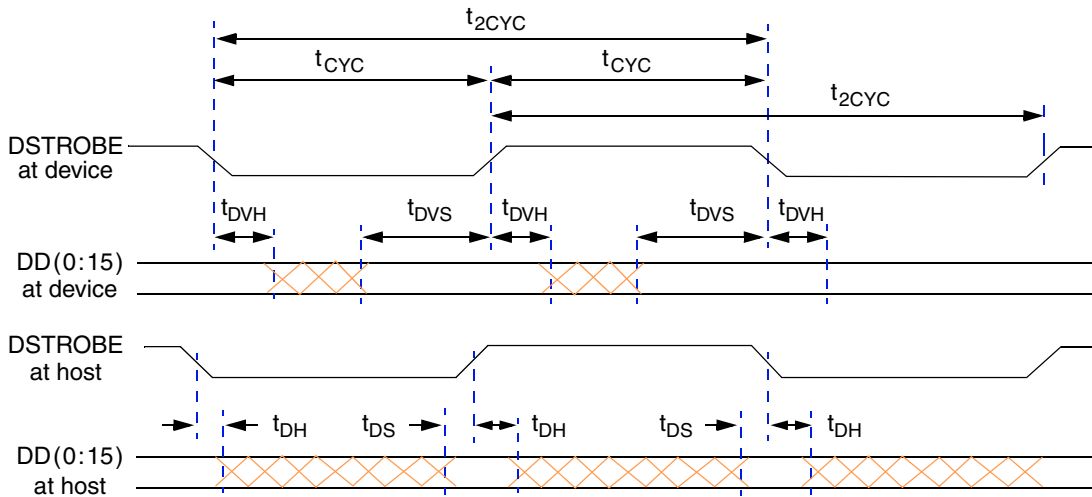


Figure 17. Timing Diagram—Sustained Ultra DMA Data In Burst

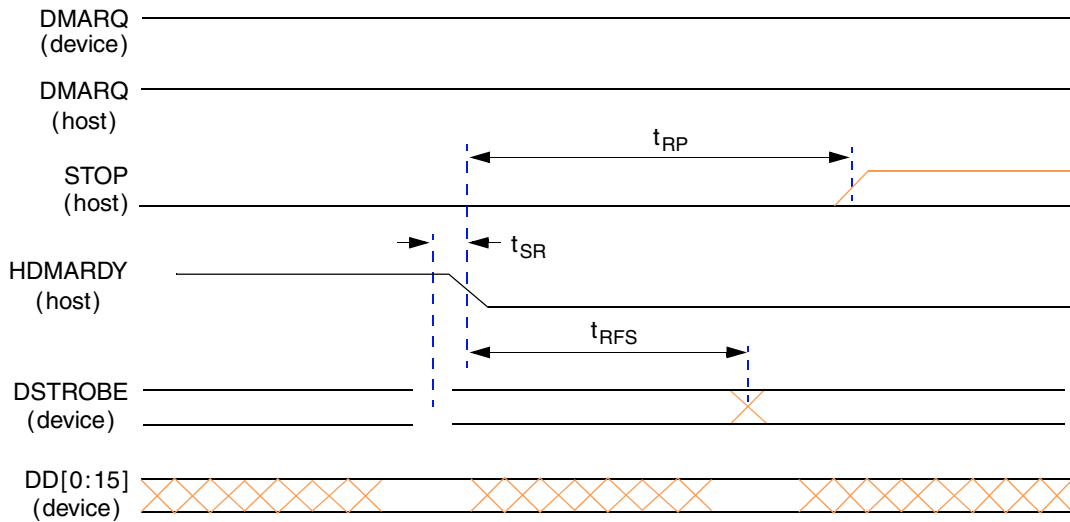


Figure 18. Timing Diagram—Host Pausing an Ultra DMA Data In Burst

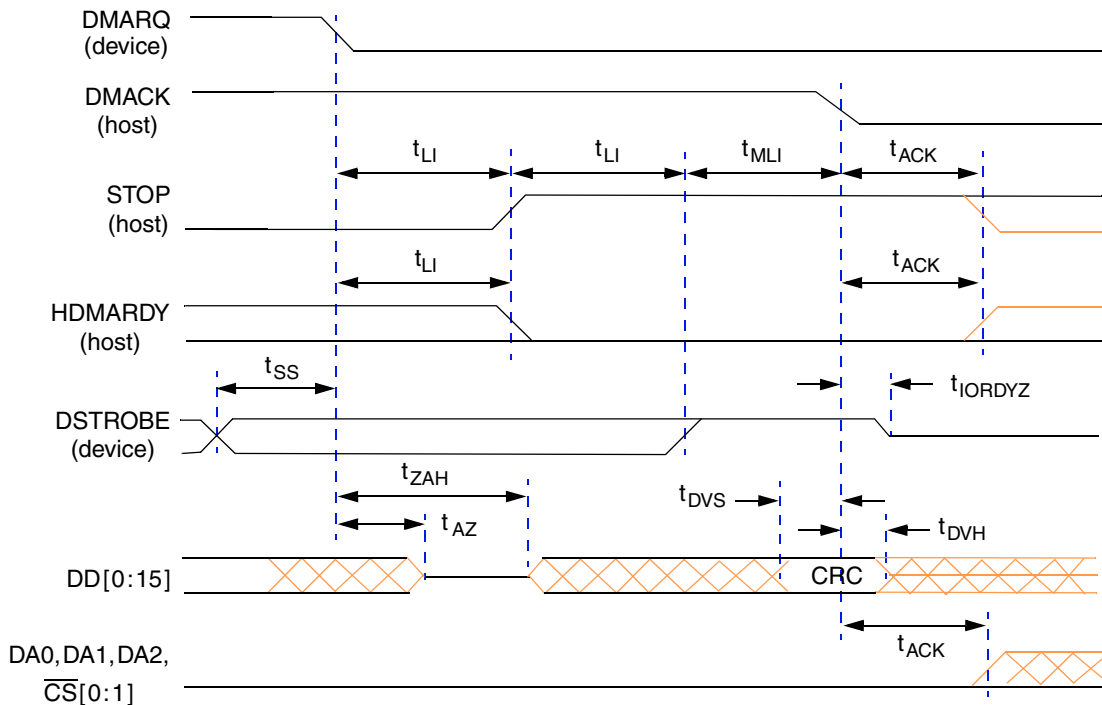


Figure 19. Timing Diagram—Drive Terminating Ultra DMA Data In Burst

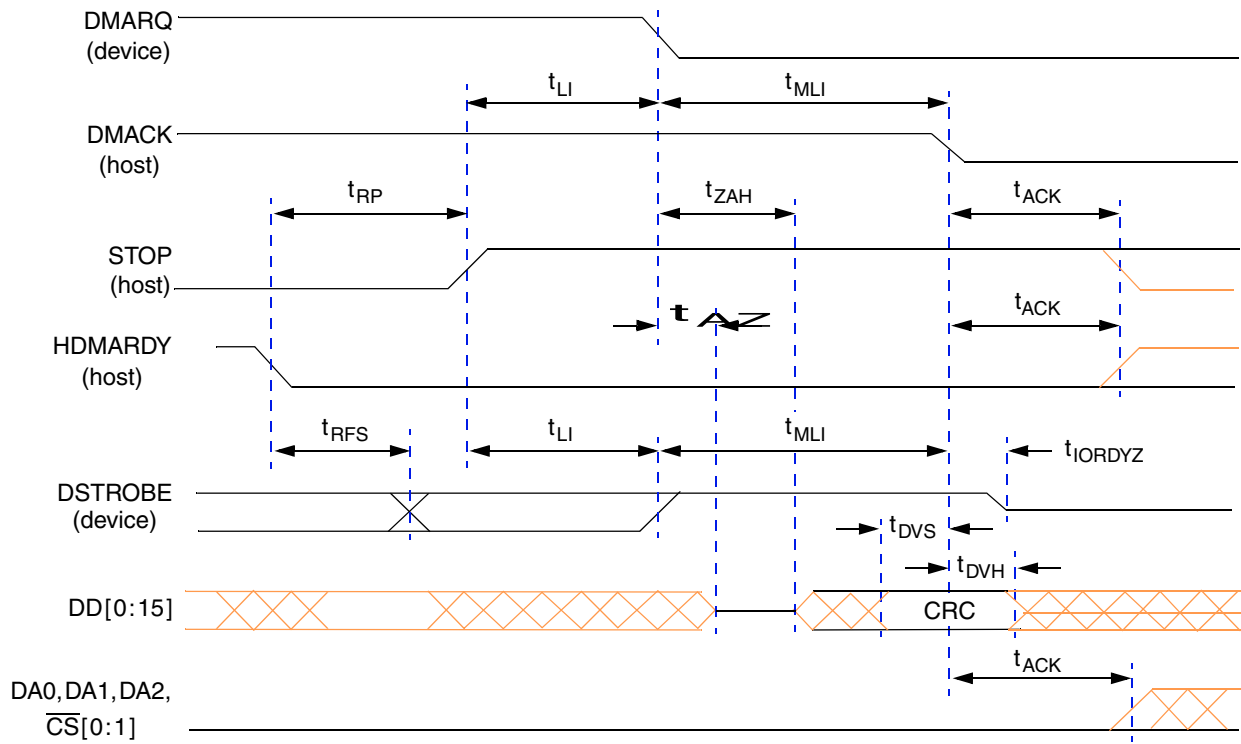


Figure 20. Timing Diagram—Host Terminating Ultra DMA Data In Burst

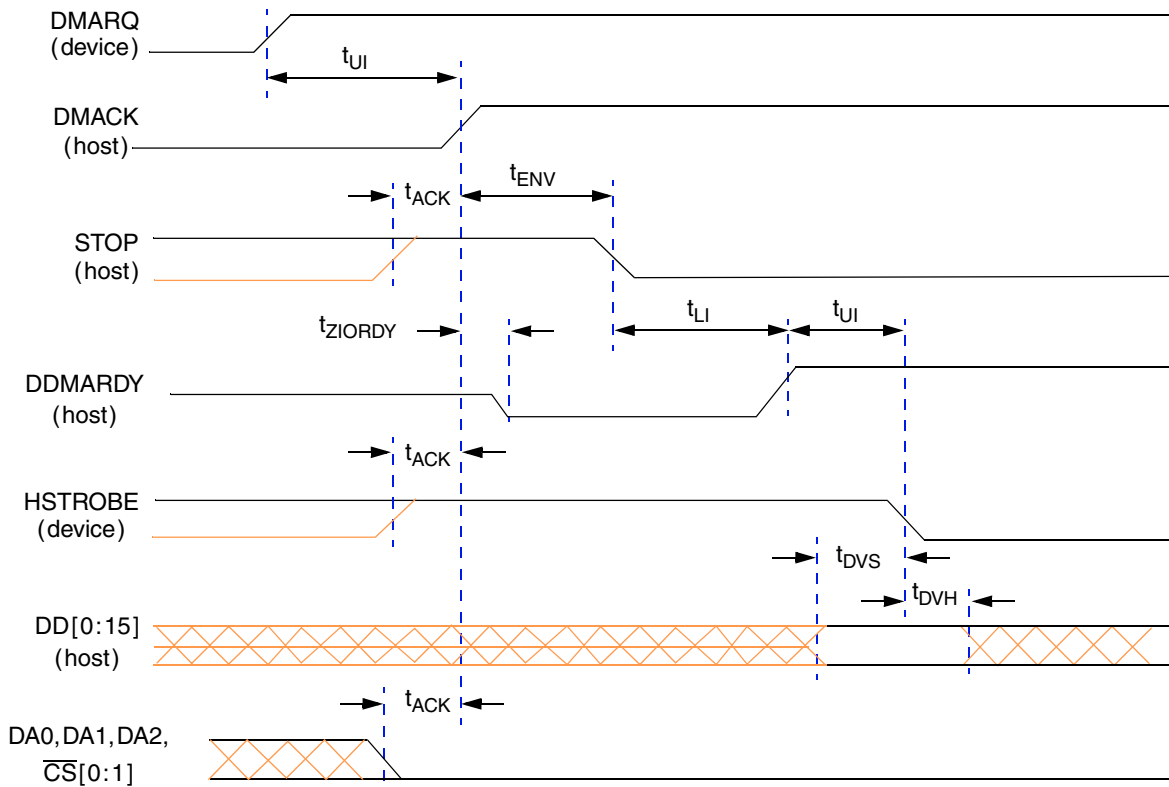


Figure 21. Timing Diagram—Initiating an Ultra DMA Data Out Burst

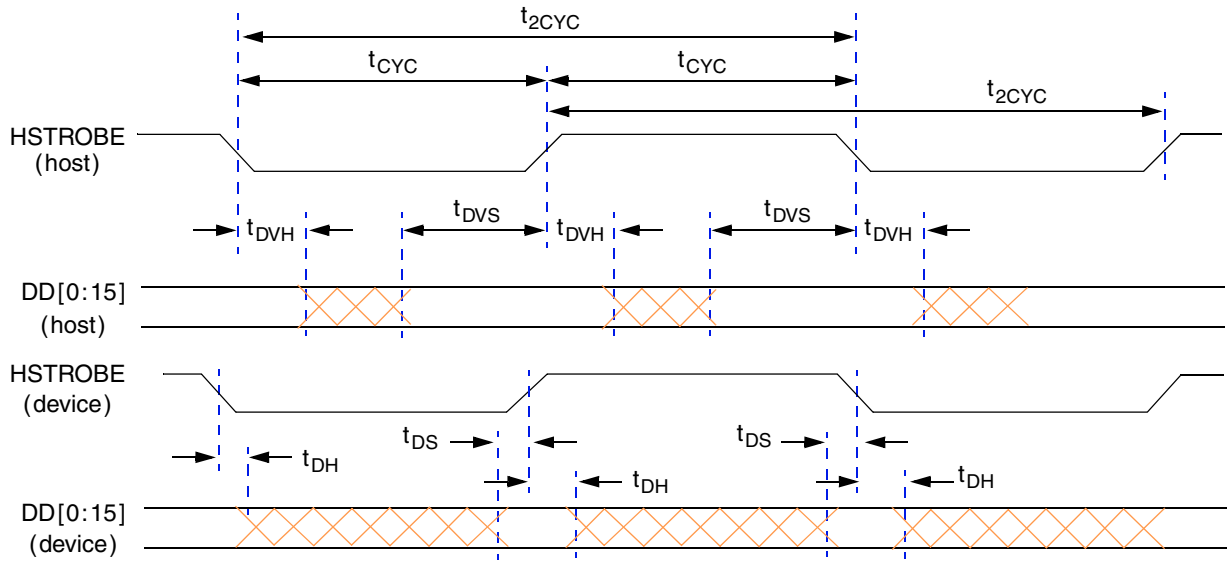


Figure 22. Timing Diagram—Sustained Ultra DMA Data Out Burst

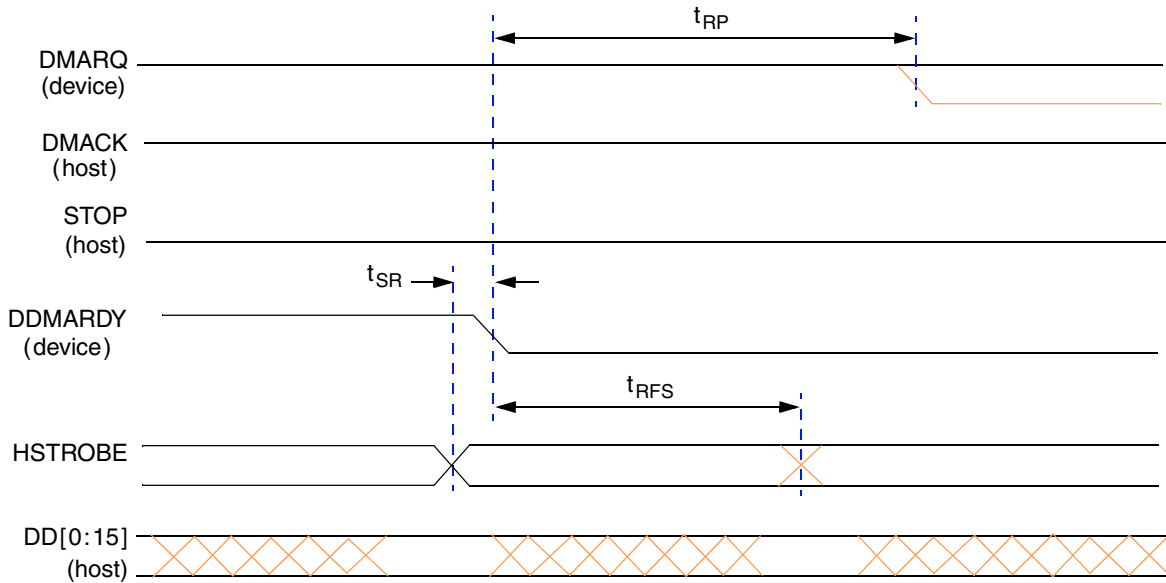


Figure 23. Timing Diagram—Drive Pausing an Ultra DMA Data Out Burst

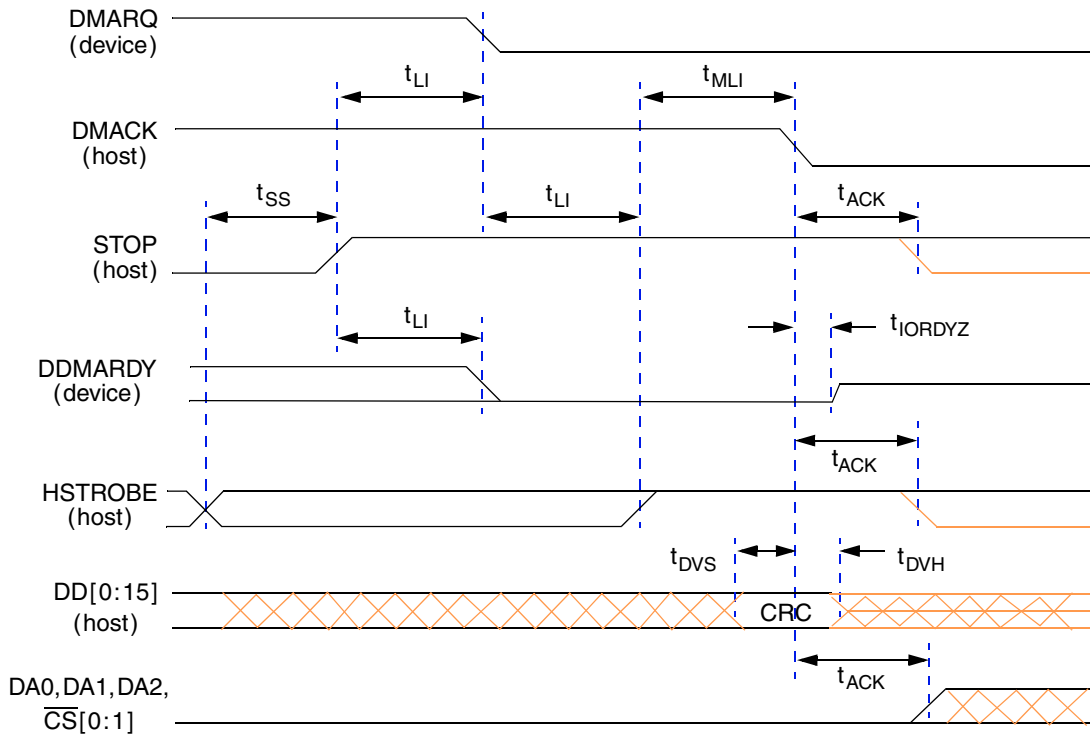


Figure 24. Timing Diagram—Host Terminating Ultra DMA Data Out Burst

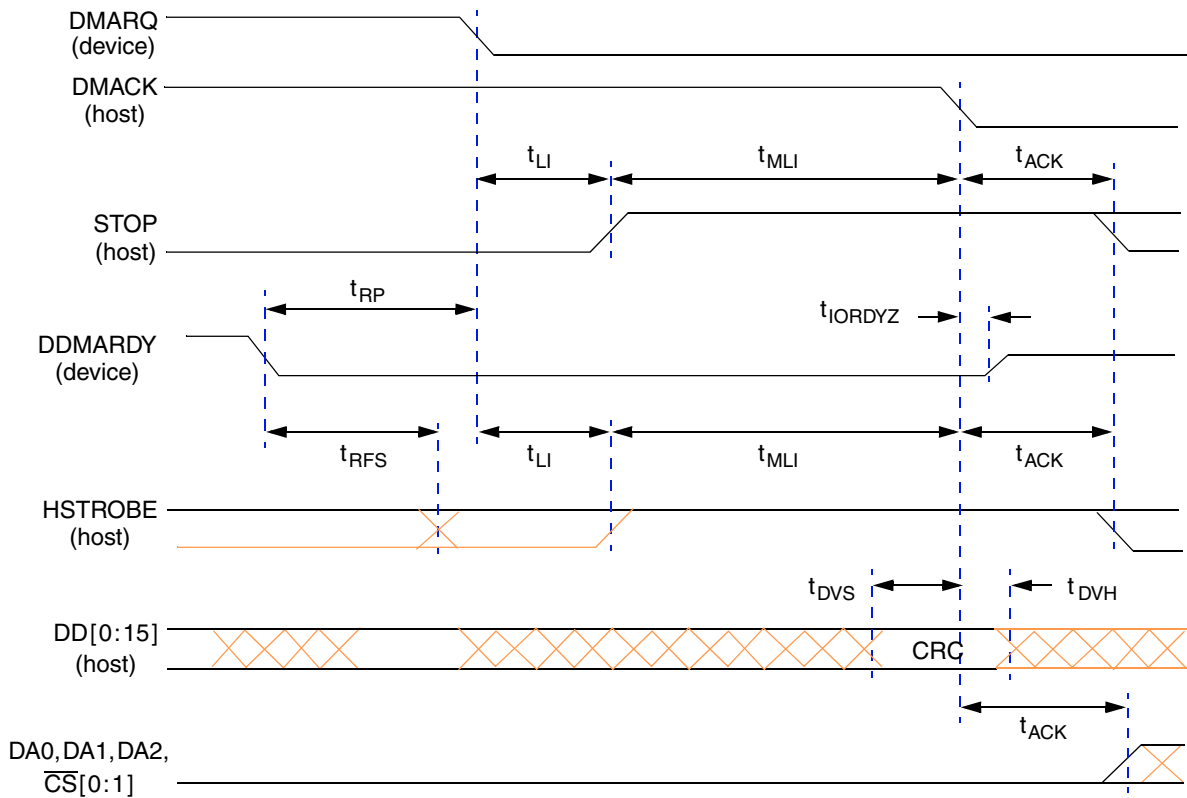


Figure 25. Timing Diagram—Drive Terminating Ultra DMA Data Out Burst

Table 30. Timing Specification ata_isolation

| Sym | Description | Min | Max | Units | SpecID |
|-----|--------------------------|-----|-----|---------------|--------|
| 1 | ata_isolation setup time | 7 | - | IP Bus cycles | A8.48 |
| 2 | ata_isolation hold time | - | 19 | IP Bus cycles | A8.49 |

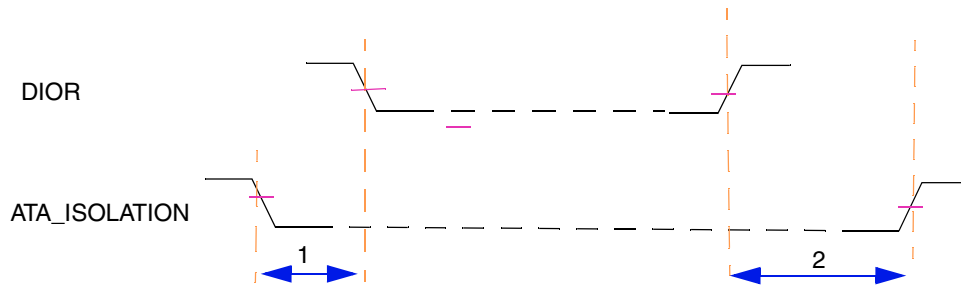


Figure 26. Timing Diagram-ATA-ISOLATION

1.3.10 Ethernet

AC Test Timing Conditions:

- Output Loading
All Outputs: 25 pF

Table 31. MII Rx Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|-------|--|-----|-----|------------------------------|--------|
| t_1 | RXD[3:0], RX_DV, RX_ER to RX_CLK setup | 10 | — | ns | A9.1 |
| t_2 | RX_CLK to RXD[3:0], RX_DV, RX_ER hold | 10 | — | ns | A9.2 |
| t_3 | RX_CLK pulse width high | 35% | 65% | RX_CLK Period ⁽¹⁾ | A9.3 |
| t_4 | RX_CLK pulse width low | 35% | 65% | RX_CLK Period ⁽¹⁾ | A9.4 |

¹ RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification.

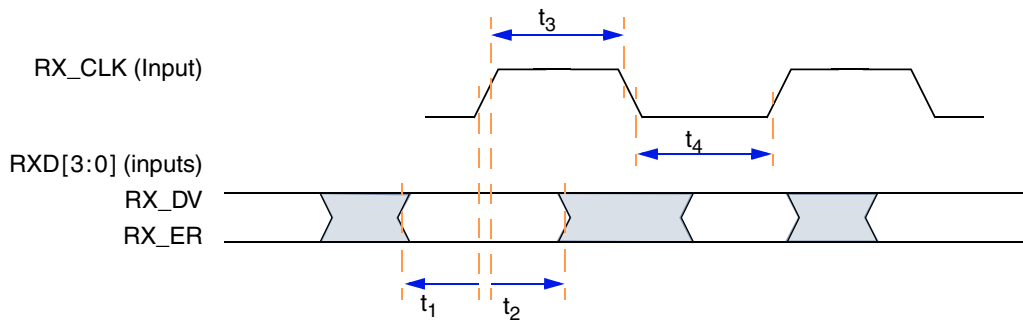


Figure 27. Ethernet Timing Diagram—MII Rx Signal

Table 32. MII Tx Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|----------------|--|-----|-----|------------------------------|--------|
| t ₅ | TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER invalid | 5 | — | ns | A9.5 |
| t ₆ | TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER valid | — | 25 | ns | A9.6 |
| t ₇ | TX_CLK pulse width high | 35% | 65% | TX_CLK Period ⁽¹⁾ | A9.7 |
| t ₈ | TX_CLK pulse width low | 35% | 65% | TX_CLK Period ⁽¹⁾ | A9.8 |

¹ The TX_CLK frequency shall be 25% of the nominal transmit frequency, e.g., a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 Specification.

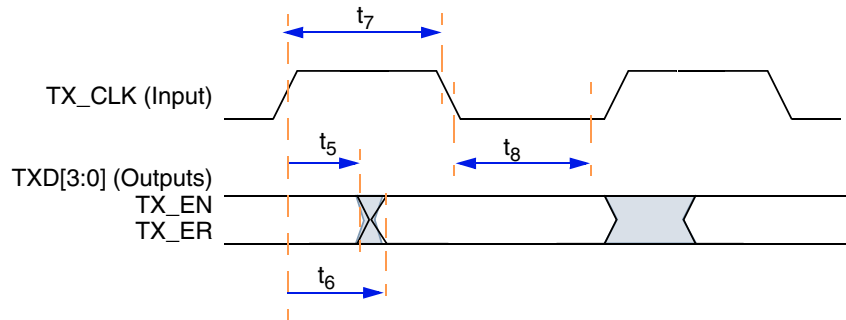


Figure 28. Ethernet Timing Diagram—MII Tx Signal

Table 33. MII Async Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|----------------|------------------------------|-----|-----|---------------|--------|
| t ₉ | CRS, COL minimum pulse width | 1.5 | — | TX_CLK Period | A9.9 |

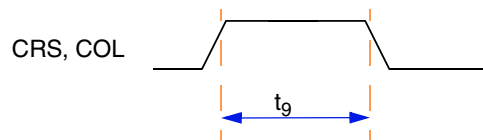


Figure 29. Ethernet Timing Diagram—MII Async

Table 34. MII Serial Management Channel Signal Timing

| Sym | Description | Min | Max | Unit | SpecID |
|-----------------|---------------------------------------|-----|-----|------|--------|
| t ₁₀ | MDC falling edge to MDIO output delay | 0 | 25 | ns | A9.10 |
| t ₁₁ | MDIO (input) to MDC rising edge setup | 10 | — | ns | A9.11 |
| t ₁₂ | MDIO (input) to MDC rising edge hold | 10 | — | ns | A9.12 |
| t ₁₃ | MDC pulse width high ⁽¹⁾ | 160 | — | ns | A9.13 |
| t ₁₄ | MDC pulse width low ⁽¹⁾ | 160 | — | ns | A9.14 |
| t ₁₅ | MDC period ⁽²⁾ | 400 | — | ns | A9.15 |

¹ MDC is generated by MPC5200B with a duty cycle of 50% except when MII_SPEED in the FEC MII_SPEED control register is changed during operation. See the MPC5200B User Manual.

² The MDC period must be set to a value of less than or equal to 2.5 MHz (to be compliant with the IEEE MII characteristic) by programming the FEC MII_SPEED control register. See the MPC5200B User Manual.

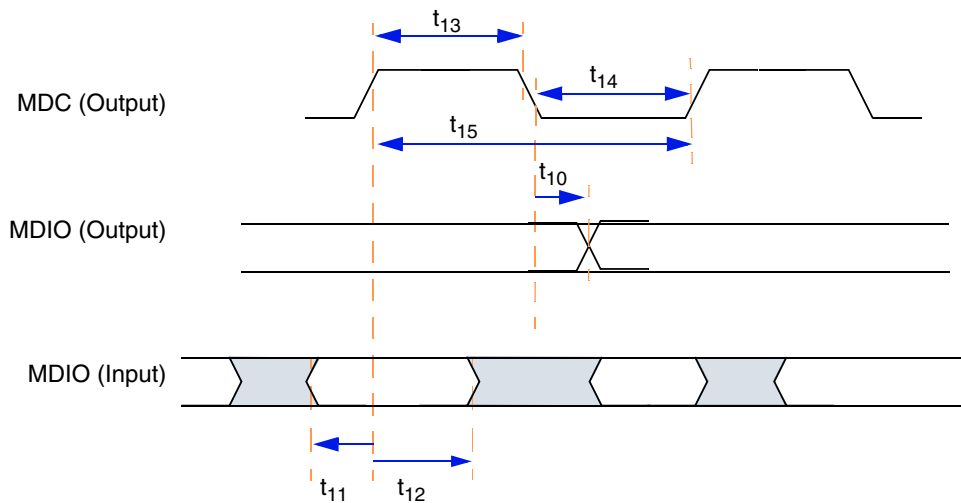


Figure 30. Ethernet Timing Diagram—MII Serial Management

1.3.11 USB

Table 35. Timing Specifications—USB Output Line

| Sym | Description | Min | Max | Units | SpecID |
|-----|------------------------------|------|-----|-------|--------|
| 1 | USB Bit width ⁽¹⁾ | 83.3 | 667 | ns | A10.1 |
| 2 | Transceiver enable time | 83.3 | 667 | ns | A10.2 |
| 3 | Signal falling time | — | 7.9 | ns | A10.3 |
| 4 | Signal rising time | — | 7.9 | ns | A10.4 |

¹ Defined in the USB config register, (12 Mbit/s or 1.5 Mbit/s mode).

NOTE

Output timing is specified at a nominal 50 pF load.

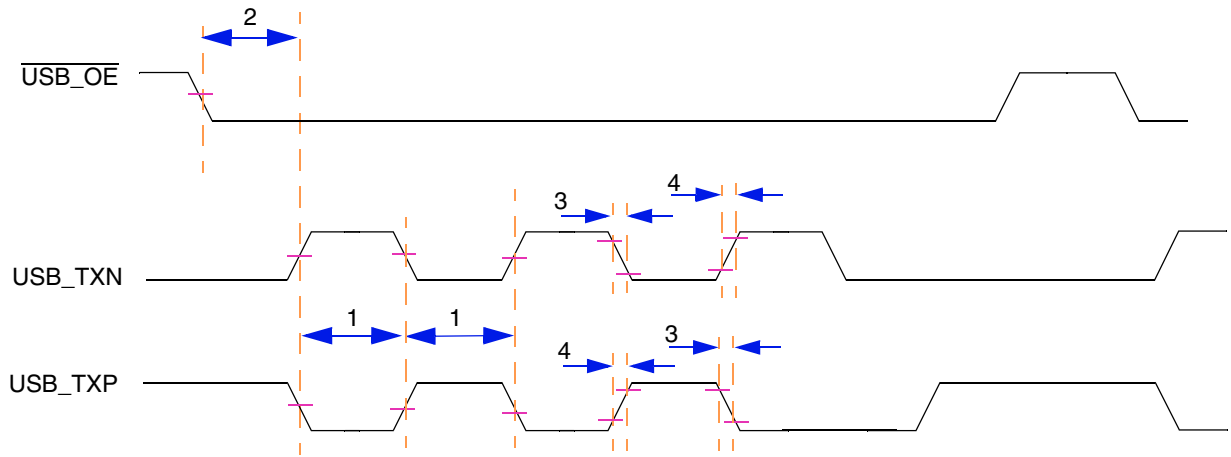


Figure 31. Timing Diagram—USB Output Line

1.3.12 SPI

Table 36. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

| Sym | Description | Min | Max | Units | SpecID |
|-----|--|------|------|-----------------------------|--------|
| 1 | Cycle time | 4 | 1024 | IP-Bus Cycle ⁽¹⁾ | A11.1 |
| 2 | Clock high or low time | 2 | 512 | IP-Bus Cycle ⁽¹⁾ | A11.2 |
| 3 | Slave select to clock delay | 15.0 | — | ns | A11.3 |
| 4 | Output Data valid after Slave Select (\overline{SS}) | — | 20.0 | ns | A11.4 |
| 5 | Output Data valid after SCK | — | 20.0 | ns | A11.5 |
| 6 | Input Data setup time | 20.0 | — | ns | A11.6 |
| 7 | Input Data hold time | 20.0 | — | ns | A11.7 |
| 8 | Slave disable lag time | 15.0 | — | ns | A11.8 |
| 9 | Sequential transfer delay | 1 | — | IP-Bus Cycle ⁽¹⁾ | A11.9 |
| 10 | Clock falling time | — | 7.9 | ns | A11.10 |
| 11 | Clock rising time | — | 7.9 | ns | A11.11 |

¹ Inter Peripheral Clock is defined in the MPC5200B User Manual.

NOTE

Output timing is specified at a nominal 50 pF load.

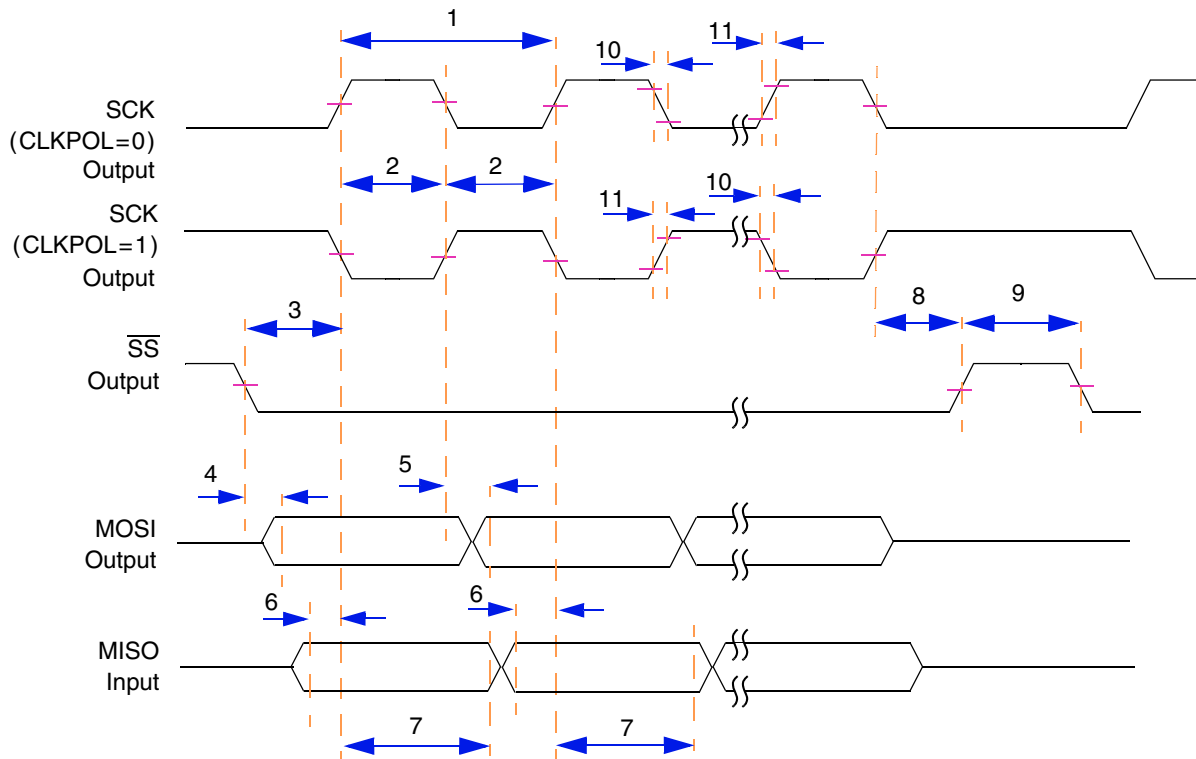


Figure 32. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 37. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

| Sym | Description | Min | Max | Units | SpecID |
|-----|--|------|------|-----------------------------|--------|
| 1 | Cycle time | 4 | 1024 | IP-Bus Cycle ⁽¹⁾ | A11.12 |
| 2 | Clock high or low time | 2 | 512 | IP-Bus Cycle ⁽¹⁾ | A11.13 |
| 3 | Slave select to clock delay | 15.0 | — | ns | A11.14 |
| 4 | Output Data valid after Slave Select (\overline{SS}) | — | 50.0 | ns | A11.15 |
| 5 | Output Data valid after SCK | — | 50.0 | ns | A11.16 |
| 6 | Input Data setup time | 50.0 | — | ns | A11.17 |
| 7 | Input Data hold time | 0.0 | — | ns | A11.18 |
| 8 | Slave disable lag time | 15.0 | — | ns | A11.19 |
| 9 | Sequential Transfer delay | 1 | — | IP-Bus Cycle ⁽¹⁾ | A11.20 |

¹ Inter Peripheral Clock is defined in the MPC5200B User Manual.

NOTE

Output timing is specified at a nominal 50 pF load.

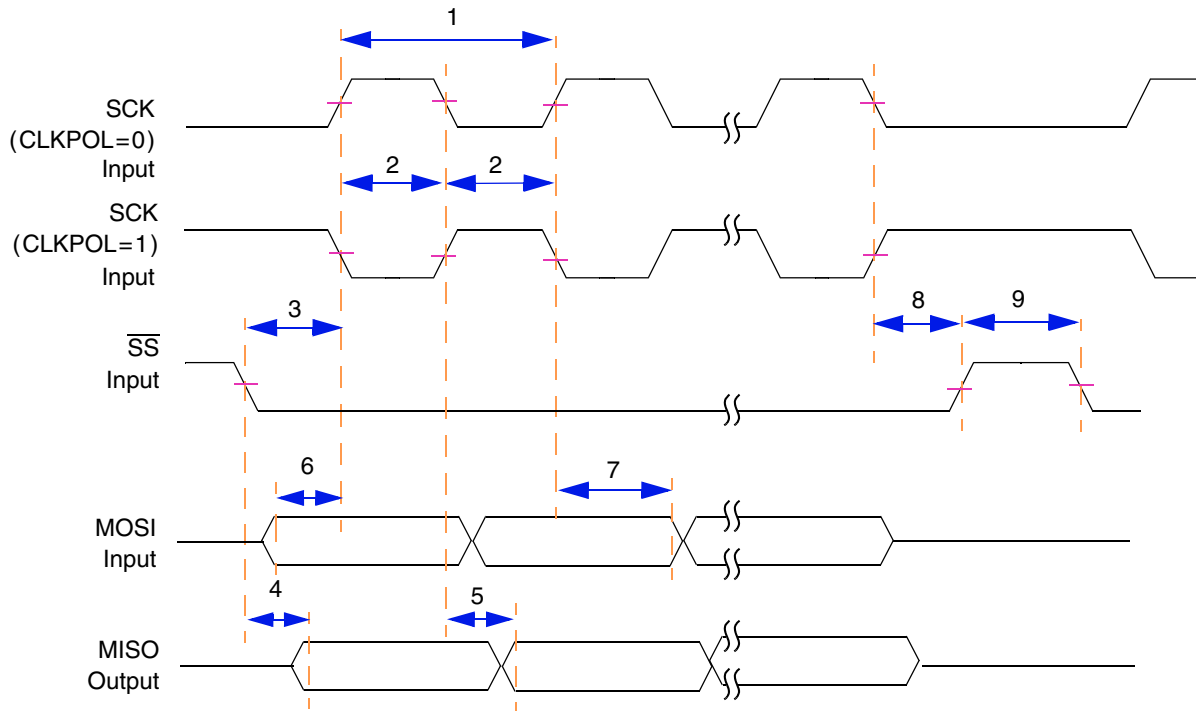


Figure 33. Timing Diagram — SPI Slave Mode, Format 0 (CPHA = 0)

Table 38. Timing Specifications — SPI Master Mode, Format 1 (CPHA = 1)

| Sym | Description | Min | Max | Units | SpecID |
|-----|-----------------------------|------|------|-----------------------------|--------|
| 1 | Cycle time | 4 | 1024 | IP-Bus Cycle ⁽¹⁾ | A11.21 |
| 2 | Clock high or low time | 2 | 512 | IP-Bus Cycle ⁽¹⁾ | A11.22 |
| 3 | Slave select to clock delay | 15.0 | — | ns | A11.23 |
| 4 | Output data valid | — | 20.0 | ns | A11.24 |
| 5 | Input Data setup time | 20.0 | — | ns | A11.25 |
| 6 | Input Data hold time | 20.0 | — | ns | A11.26 |
| 7 | Slave disable lag time | 15.0 | — | ns | A11.27 |
| 8 | Sequential Transfer delay | 1 | — | IP-Bus Cycle ⁽¹⁾ | A11.28 |
| 9 | Clock falling time | — | 7.9 | ns | A11.29 |
| 10 | Clock rising time | — | 7.9 | ns | A11.30 |

¹ Inter Peripheral Clock is defined in the MPC5200B User Manual.

NOTE

Output timing is specified at a nominal 50 pF load.

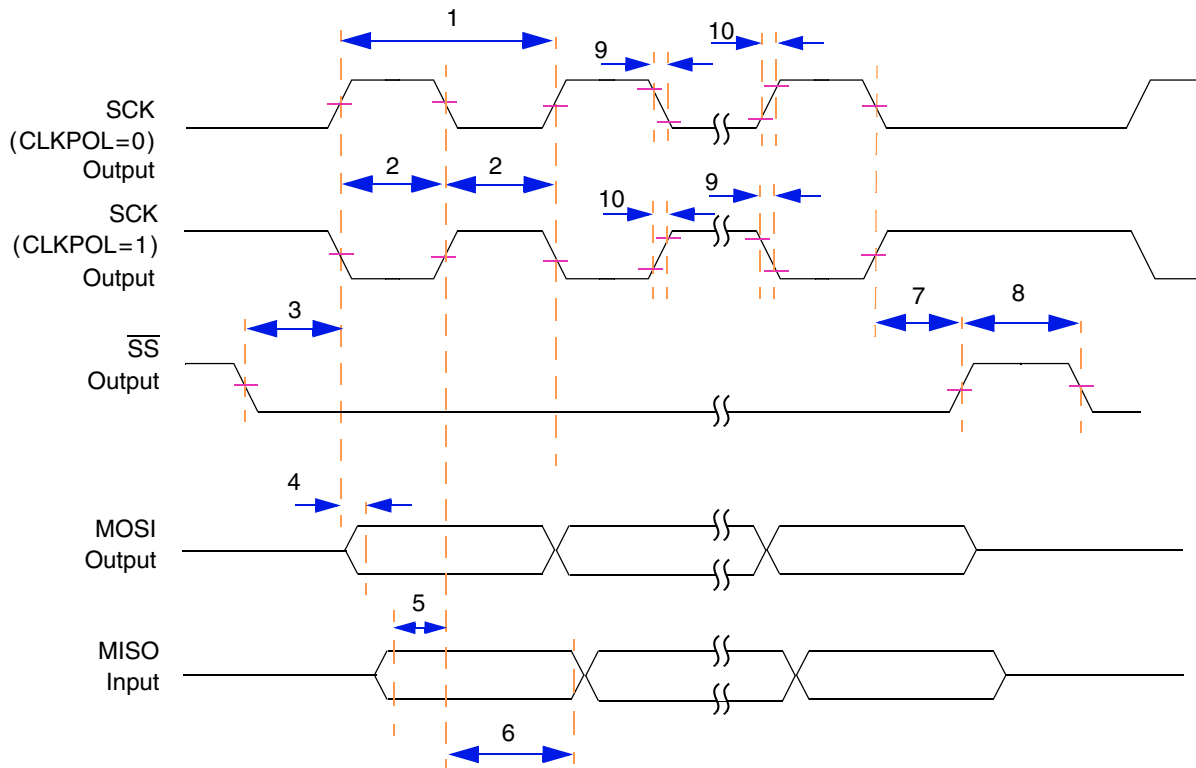


Figure 34. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 39. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

| Sym | Description | Min | Max | Units | SpecID |
|-----|-----------------------------|------|------|-----------------------------|--------|
| 1 | Cycle time | 4 | 1024 | IP-Bus Cycle ⁽¹⁾ | A11.31 |
| 2 | Clock high or low time | 2 | 512 | IP-Bus Cycle ⁽¹⁾ | A11.32 |
| 3 | Slave select to clock delay | 15.0 | — | ns | A11.33 |
| 4 | Output data valid | — | 50.0 | ns | A11.34 |
| 5 | Input Data setup time | 50.0 | — | ns | A11.35 |
| 6 | Input Data hold time | 0.0 | — | ns | A11.36 |
| 7 | Slave disable lag time | 15.0 | — | ns | A11.37 |
| 8 | Sequential Transfer delay | 1 | — | IP-Bus Cycle ⁽¹⁾ | A11.38 |

¹ Inter Peripheral Clock is defined in the MPC5200B User Manual.

NOTE

Output timing is specified at a nominal 50 pF load.

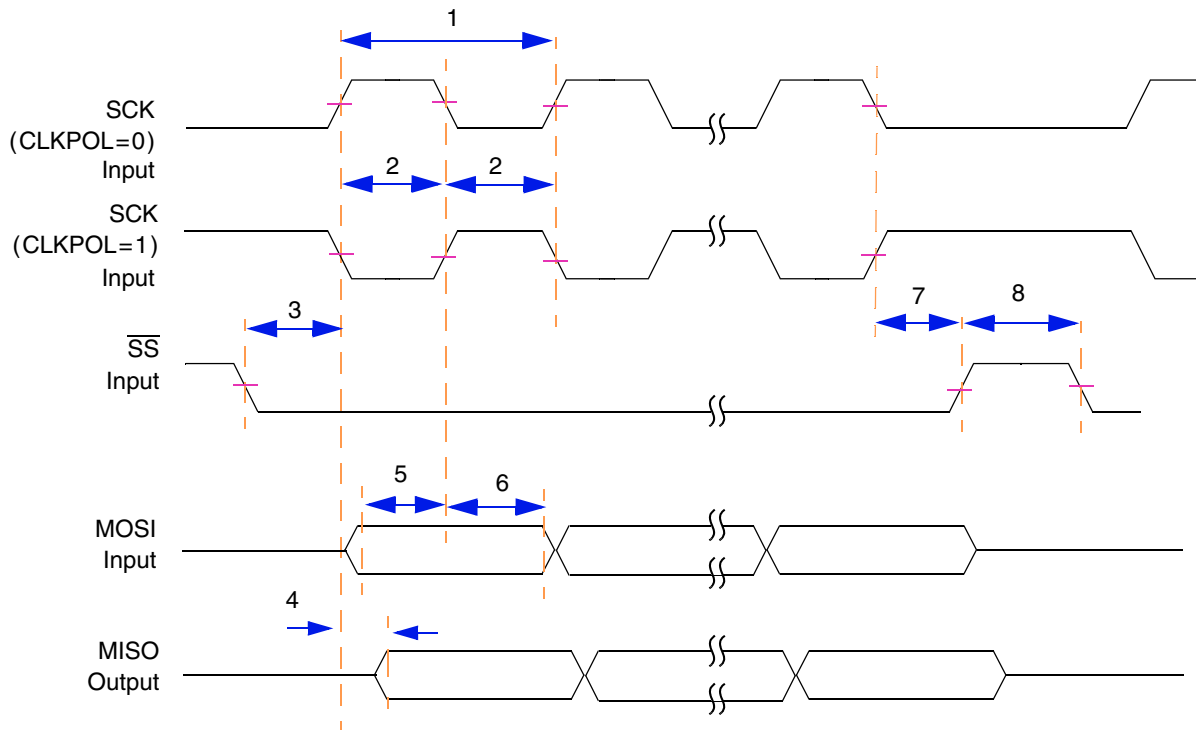


Figure 35. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

1.3.13 MSCAN

The CAN functions are available as RX and TX pins at normal IO pads (I²C1+GPTimer or PSC2). There is no filter for the WakeUp dominant pulse. Any High-to-Low edge can cause WakeUp, if configured.

1.3.14 I²C

Table 40. I²C Input Timing Specifications—SCL and SDA

| Sym | Description | Min | Max | Units | SpecID |
|-----|--|-----|-----|-----------------------------|--------|
| 1 | Start condition hold time | 2 | — | IP-Bus Cycle ⁽¹⁾ | A13.1 |
| 2 | Clock low time | 8 | — | IP-Bus Cycle ⁽¹⁾ | A13.2 |
| 4 | Data hold time | 0.0 | — | ns | A13.3 |
| 6 | Clock high time | 4 | — | IP-Bus Cycle ⁽¹⁾ | A13.4 |
| 7 | Data setup time | 0.0 | — | ns | A13.5 |
| 8 | Start condition setup time (for repeated start condition only) | 2 | — | IP-Bus Cycle ⁽¹⁾ | A13.6 |
| 9 | Stop condition setup time | 2 | — | IP-Bus Cycle ⁽¹⁾ | A13.7 |

¹ Inter Peripheral Clock is defined in the MPC5200B User Manual.

Table 41. I²C Output Timing Specifications—SCL and SDA

| Sym | Description | Min | Max | Units | SpecID |
|------------------|--|-----|-----|-----------------------------|--------|
| 1 ⁽¹⁾ | Start condition hold time | 6 | — | IP-Bus Cycle ⁽³⁾ | A13.8 |
| 2 ⁽¹⁾ | Clock low time | 10 | — | IP-Bus Cycle ⁽³⁾ | A13.9 |
| 3 ⁽²⁾ | SCL/SDA rise time | — | 7.9 | ns | A13.10 |
| 4 ⁽¹⁾ | Data hold time | 7 | — | IP-Bus Cycle ⁽³⁾ | A13.11 |
| 5 ⁽¹⁾ | SCL/SDA fall time | — | 7.9 | ns | A13.12 |
| 6 ⁽¹⁾ | Clock high time | 10 | — | IP-Bus Cycle ⁽³⁾ | A13.13 |
| 7 ⁽¹⁾ | Data setup time | 2 | — | IP-Bus Cycle ⁽³⁾ | A13.14 |
| 8 ⁽¹⁾ | Start condition setup time (for repeated start condition only) | 20 | — | IP-Bus Cycle ⁽³⁾ | A13.15 |
| 9 ⁽¹⁾ | Stop condition setup time | 10 | — | IP-Bus Cycle ⁽³⁾ | A13.16 |

¹ Programming IFDR with the maximum frequency (IFDR=0x20) results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

² Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values

³ Inter Peripheral Clock is defined in the MPC5200B User Manual.

NOTE

Output timing is specified at a nominal 50 pF load.

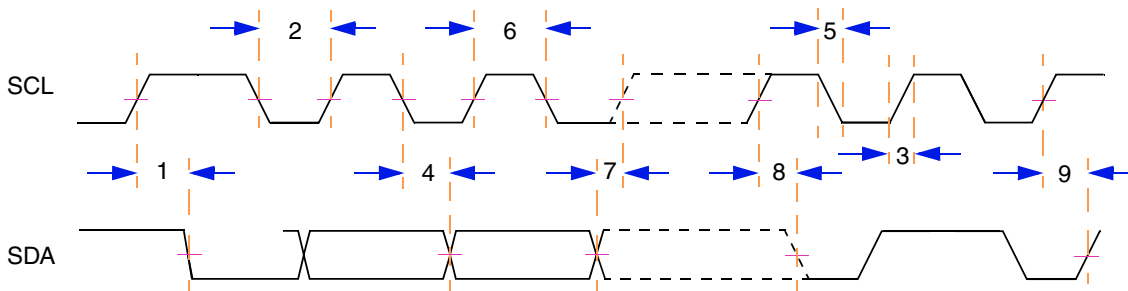


Figure 36. Timing Diagram—I²C Input/Output

1.3.15 J1850

See the MPC5200B User Manual.

1.3.16 PSC

1.3.16.1 Codec Mode (8,16,24 and 32-bit)/I²S Mode

Table 42. Timing Specifications—8,16, 24, and 32-bit CODEC / I²S Master Mode

| Sym | Description | Min | Typ | Max | Units | SpecID |
|-----|--|------|-----|-----|------------------|--------|
| 1 | Bit Clock cycle time, programmed in CCS register | 40.0 | — | — | ns | A15.1 |
| 2 | Clock duty cycle | — | 50 | — | % ⁽¹⁾ | A15.2 |
| 3 | Bit Clock fall time | — | — | 7.9 | ns | A15.3 |
| 4 | Bit Clock rise time | — | — | 7.9 | ns | A15.4 |
| 5 | FrameSync valid after clock edge | — | — | 8.4 | ns | A15.5 |
| 6 | FrameSync invalid after clock edge | — | — | 8.4 | ns | A15.6 |
| 7 | Output Data valid after clock edge | — | — | 9.3 | ns | A15.7 |
| 8 | Input Data setup time | 6.0 | — | — | ns | A15.8 |

¹ Bit Clock cycle time

NOTE

Output timing is specified at a nominal 50 pF load.

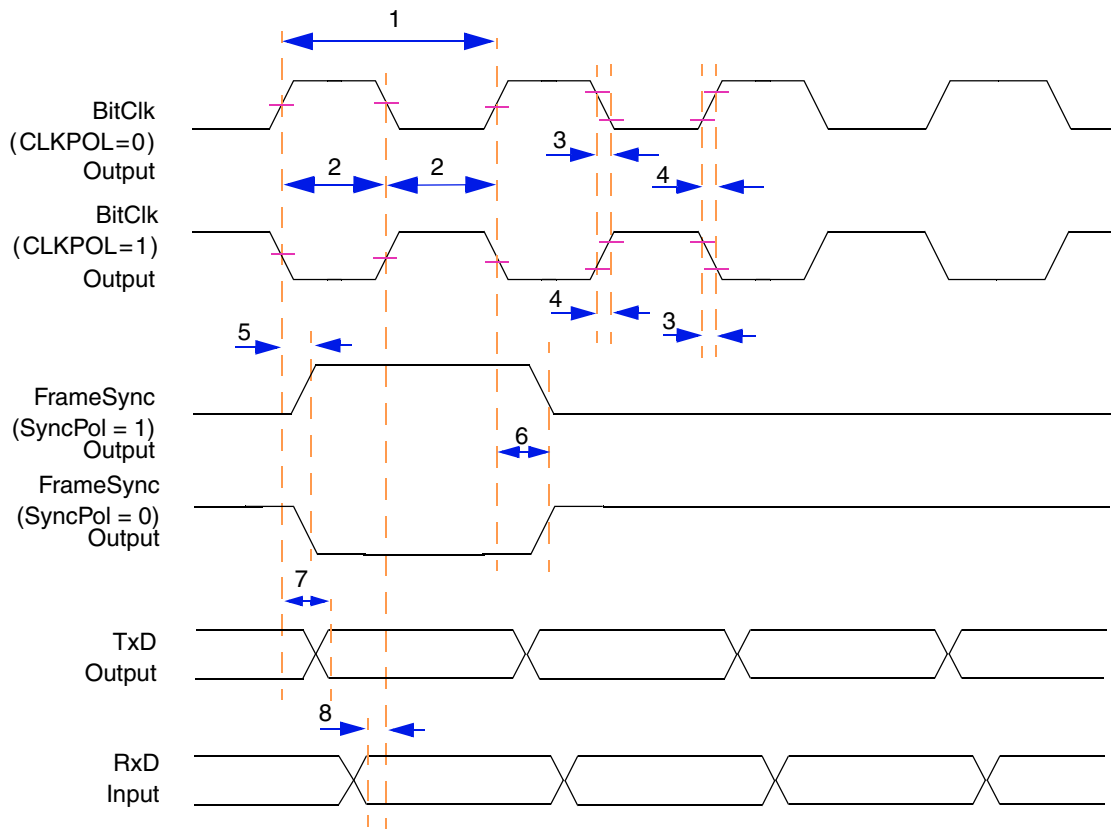


Figure 37. Timing Diagram — 8,16, 24, and 32-bit CODEC / I²S Master Mode

Table 43. Timing Specifications — 8,16, 24, and 32-bit CODEC / I²S Slave Mode

| Sym | Description | Min | Typ | Max | Units | SpecID |
|-----|------------------------------------|------|-----|------|------------------|--------|
| 1 | Bit Clock cycle time | 40.0 | — | — | ns | A15.9 |
| 2 | Clock duty cycle | — | 50 | — | % ⁽¹⁾ | A15.10 |
| 3 | FrameSync setup time | 1.0 | — | — | ns | A15.11 |
| 4 | Output Data valid after clock edge | — | — | 14.0 | ns | A15.12 |
| 5 | Input Data setup time | 1.0 | — | — | ns | A15.13 |
| 6 | Input Data hold time | 1.0 | — | — | ns | A15.14 |

¹ Bit Clock cycle time

NOTE

Output timing is specified at a nominal 50 pF load.

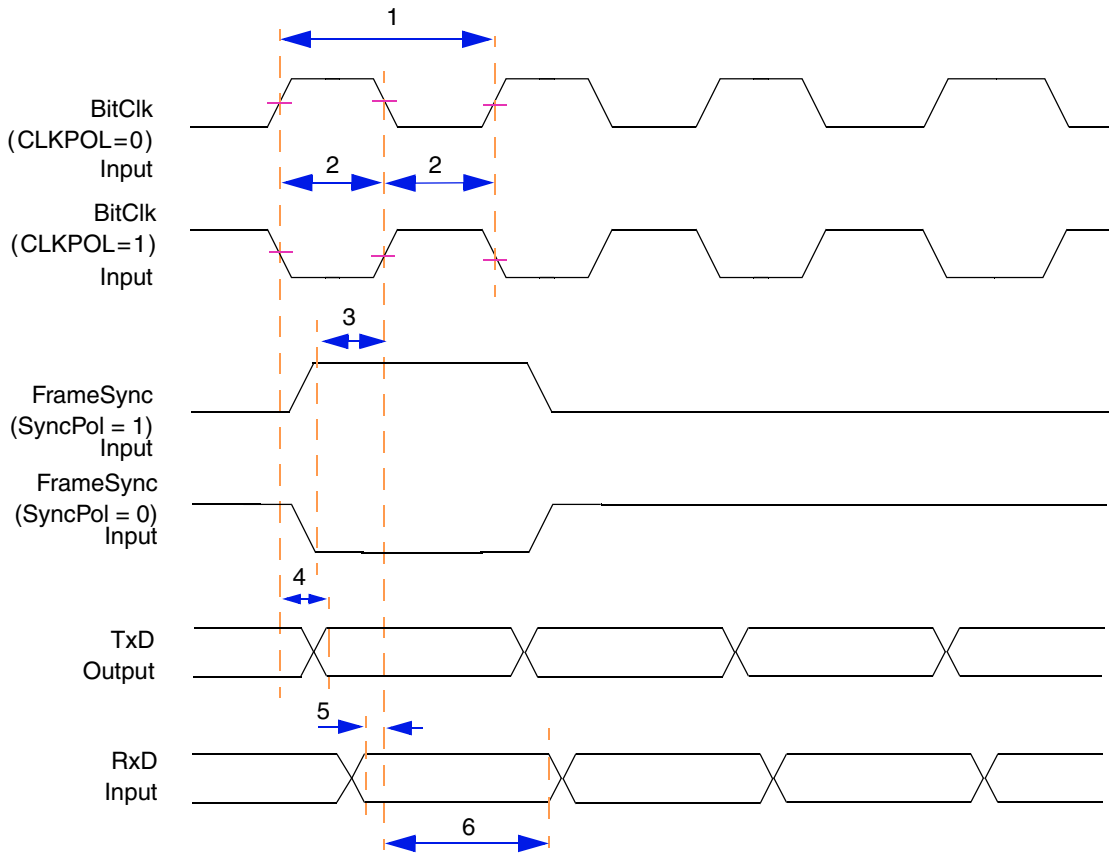


Figure 38. Timing Diagram — 8,16, 24, and 32-bit CODEC / I²S Slave Mode

1.3.16.2 AC97 Mode

Table 44. Timing Specifications — AC97 Mode

| Sym | Description | Min | Typ | Max | Units | SpecID |
|-----|---|-----|------|------|-------|--------|
| 1 | Bit Clock cycle time | — | 81.4 | — | ns | A15.15 |
| 2 | Clock pulse high time | — | 40.7 | — | ns | A15.16 |
| 3 | Clock pulse low time | — | 40.7 | — | ns | A15.17 |
| 4 | FrameSync valid after rising clock edge | — | — | 13.0 | ns | A15.18 |
| 5 | Output Data valid after rising clock edge | — | — | 14.0 | ns | A15.19 |
| 6 | Input Data setup time | 1.0 | — | — | ns | A15.20 |
| 7 | Input Data hold time | 1.0 | — | — | ns | A15.21 |

NOTE

Output timing is specified at a nominal 50 pF load.

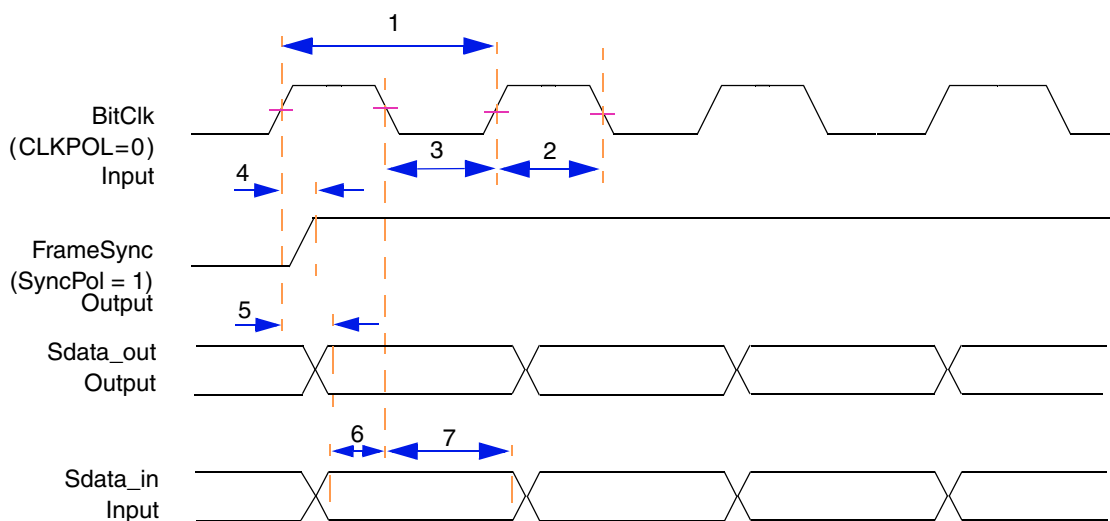


Figure 39. Timing Diagram — AC97 Mode

1.3.16.3 IrDA Mode

Table 45. Timing Specifications — IrDA Transmit Line

| Sym | Description | Min | Max | Units | SpecID |
|-----|--|-------|-------|-------|--------|
| 1 | Pulse high time, defined in the IrDA protocol definition | 0.125 | 10000 | μs | A15.22 |
| 2 | Pulse low time, defined in the IrDA protocol definition | 0.125 | 10000 | μs | A15.23 |
| 3 | Transmitter rising time | — | 7.9 | ns | A15.24 |
| 4 | Transmitter falling time | — | 7.9 | ns | A15.25 |

NOTE

Output timing is specified at a nominal 50 pF load.

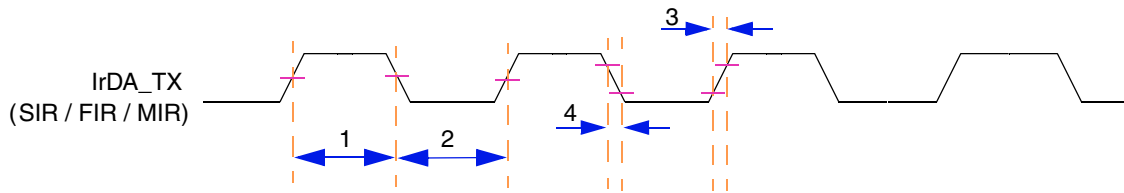


Figure 40. Timing Diagram — IrDA Transmit Line

1.3.16.4 SPI Mode

Table 46. Timing Specifications — SPI Master Mode, Format 0 (CPHA = 0)

| Sym | Description | Min | Max | Units | SpecID |
|-----|---|------|-----|-------|--------|
| 1 | SCK cycle time, programmable in the PSC CCS register | 30.0 | — | ns | A15.26 |
| 2 | SCK pulse width, 50% SCK duty cycle | 15.0 | — | ns | A15.27 |
| 3 | Slave select clock delay, programmable in the PSC CCS register | 30.0 | — | ns | A15.28 |
| 4 | Output Data valid after Slave Select (\overline{SS}) | — | 8.9 | ns | A15.29 |
| 5 | Output Data valid after SCK | — | 8.9 | ns | A15.30 |
| 6 | Input Data setup time | 6.0 | — | ns | A15.31 |
| 7 | Input Data hold time | 1.0 | — | ns | A15.32 |
| 8 | Slave disable lag time | — | 8.9 | ns | A15.33 |
| 9 | Sequential Transfer delay, programmable in the PSC CTUR / CTLR register | 15.0 | — | ns | A15.34 |
| 10 | Clock falling time | — | 7.9 | ns | A15.35 |
| 11 | Clock rising time | — | 7.9 | ns | A15.36 |

NOTE

Output timing is specified at a nominal 50 pF load.

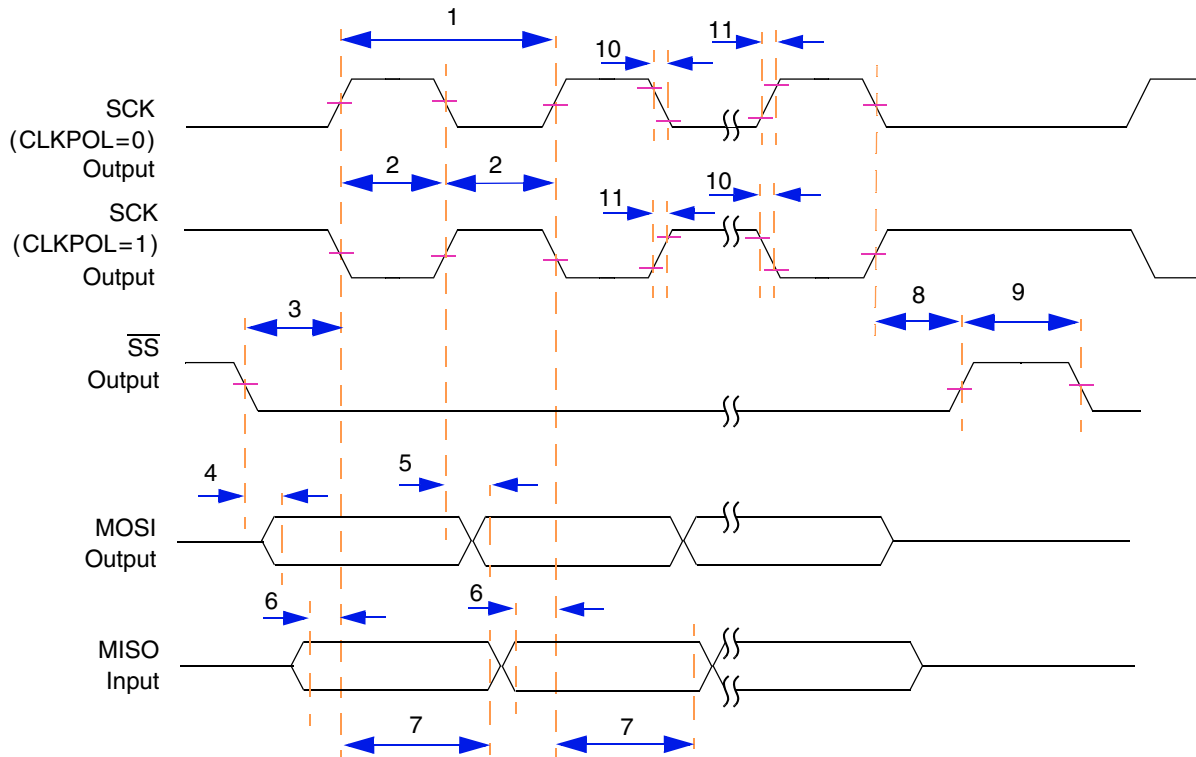


Figure 41. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 47. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0)

| Sym | Description | Min | Max | Units | SpecID |
|-----|---|------|------|-------|--------|
| 1 | SCK cycle time, programable in the PSC CCS register | 30.0 | — | ns | A15.37 |
| 2 | SCK pulse width, 50% SCK duty cycle | 15.0 | — | ns | A15.38 |
| 3 | Slave select clock delay | 1.0 | — | ns | A15.39 |
| 4 | Input Data setup time | 1.0 | — | ns | A15.40 |
| 5 | Input Data hold time | 1.0 | — | ns | A15.41 |
| 6 | Output data valid after \overline{SS} | — | 14.0 | ns | A15.42 |
| 7 | Output data valid after SCK | — | 14.0 | ns | A15.43 |
| 8 | Slave disable lag time | 0.0 | — | ns | A15.44 |
| 9 | Minimum Sequential Transfer delay = 2 * IP Bus clock cycle time | 30.0 | — | — | A15.45 |

NOTE

Output timing is specified at a nominal 50 pF load.

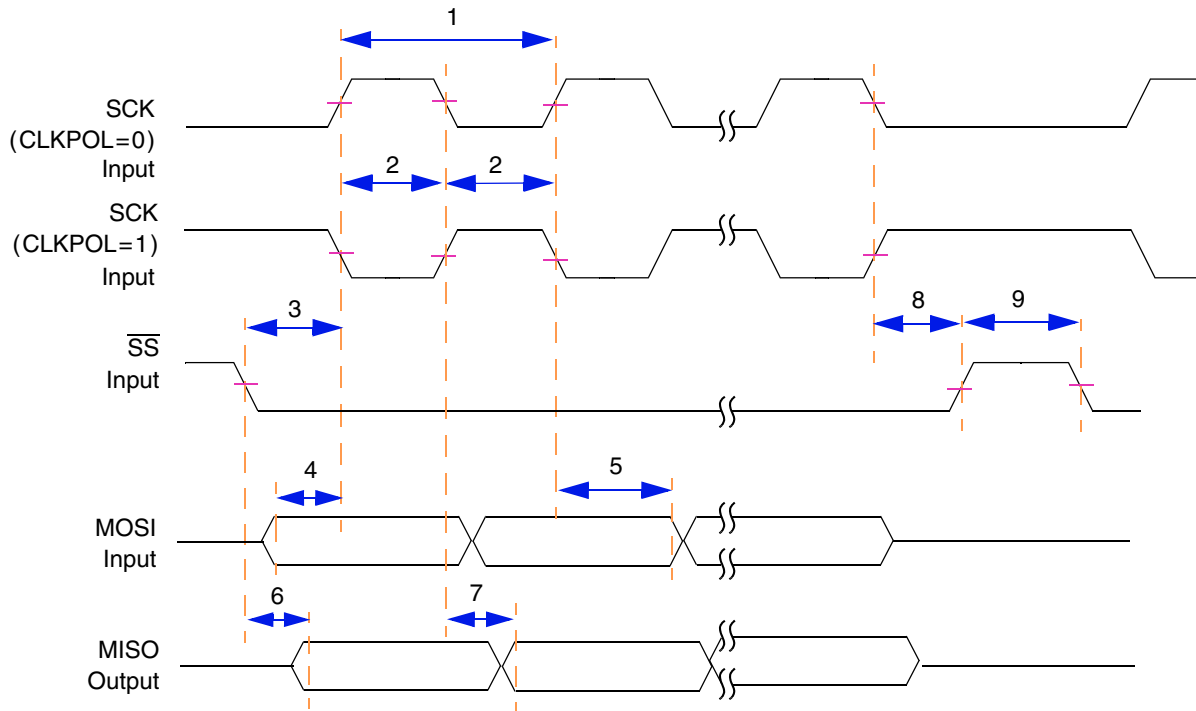


Figure 42. Timing Diagram — SPI Slave Mode, Format 0 (CPHA = 0)

Table 48. Timing Specifications — SPI Master Mode, Format 1 (CPHA = 1)

| Sym | Description | Min | Max | Units | SpecID |
|-----|---|------|-----|-------|--------|
| 1 | SCK cycle time, programmable in the PSC CCS register | 30.0 | — | ns | A15.46 |
| 2 | SCK pulse width, 50% SCK duty cycle | 15.0 | — | ns | A15.47 |
| 3 | Slave select clock delay, programmable in the PSC CCS register | 30.0 | — | ns | A15.48 |
| 4 | Output data valid | — | 8.9 | ns | A15.49 |
| 5 | Input Data setup time | 6.0 | — | ns | A15.50 |
| 6 | Input Data hold time | 1.0 | — | ns | A15.51 |
| 7 | Slave disable lag time | — | 8.9 | ns | A15.52 |
| 8 | Sequential Transfer delay, programmable in the PSC CTUR / CTRL register | 15.0 | — | ns | A15.53 |
| 9 | Clock falling time | — | 7.9 | ns | A15.54 |
| 10 | Clock rising time | — | 7.9 | ns | A15.55 |

NOTE

Output timing is specified at a nominal 50 pF load.

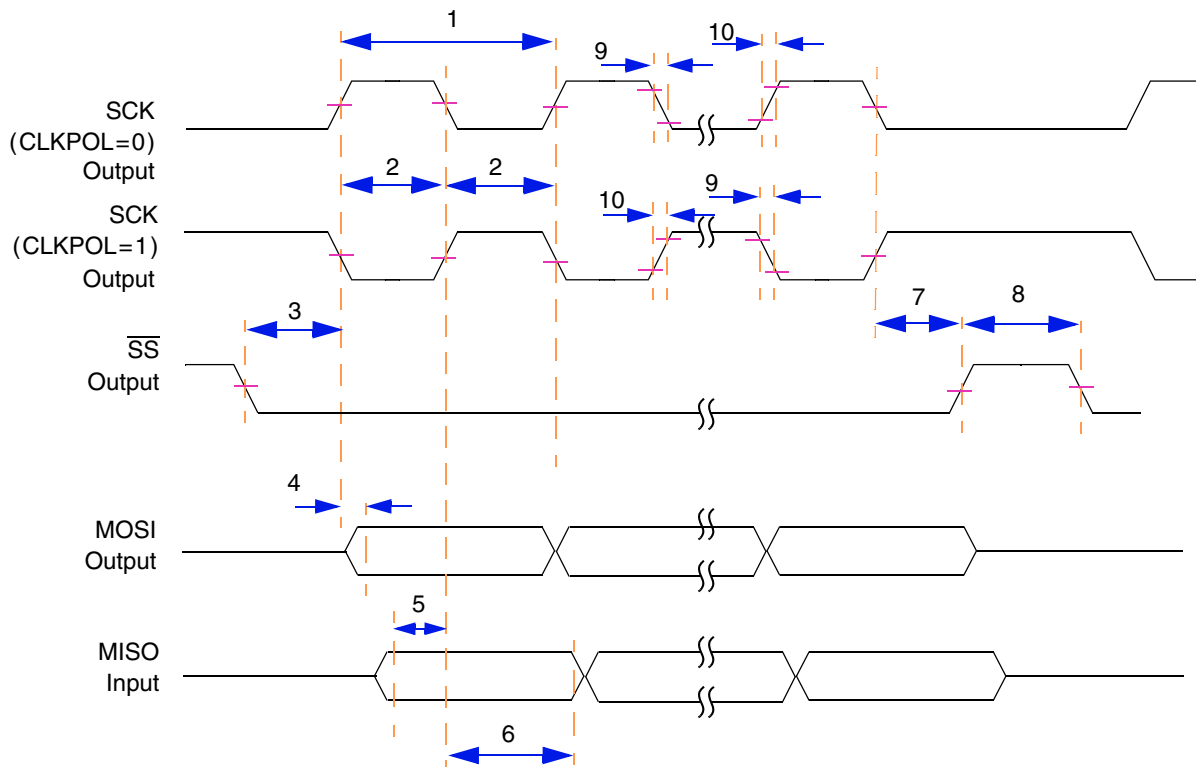


Figure 43. Timing Diagram — SPI Master Mode, Format 1 (CPHA = 1)

Table 49. Timing Specifications — SPI Slave Mode, Format 1 (CPHA = 1)

| Sym | Description | Min | Max | Units | SpecID |
|-----|---|------|------|-------|--------|
| 1 | SCK cycle time, programmable in the PSC CCS register | 30.0 | — | ns | A15.56 |
| 2 | SCK pulse width, 50% SCK duty cycle | 15.0 | — | ns | A15.57 |
| 3 | Slave select clock delay | 0.0 | — | ns | A15.58 |
| 4 | Output data valid | — | 14.0 | ns | A15.59 |
| 5 | Input Data setup time | 2.0 | — | ns | A15.60 |
| 6 | Input Data hold time | 1.0 | — | ns | A15.61 |
| 7 | Slave disable lag time | 0.0 | — | ns | A15.62 |
| 8 | Minimum Sequential Transfer delay = 2 * IP-Bus clock cycle time | 30.0 | — | ns | A15.63 |

NOTE

Output timing is specified at a nominal 50 pF load.

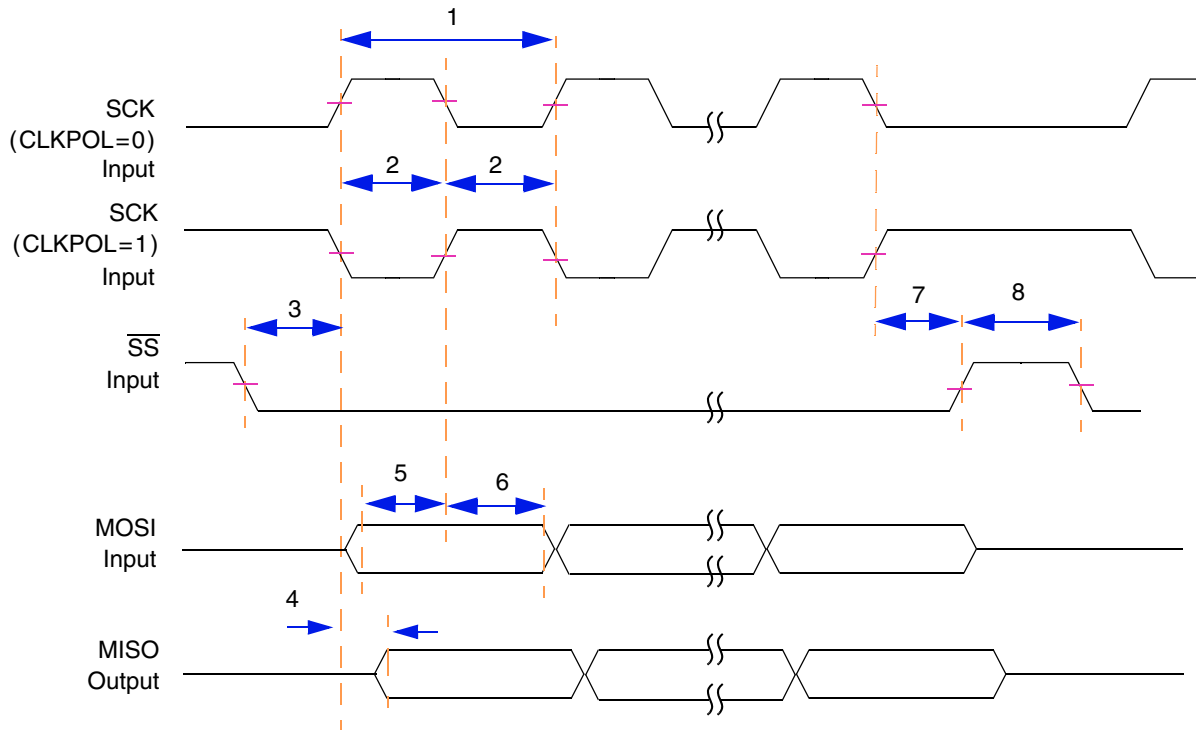


Figure 44. Timing Diagram — SPI Slave Mode, Format 1 (CPHA = 1)

1.3.17 GPIOs and Timers

1.3.17.1 General and Asynchronous Signals

The MPC5200B contains several sets of I/Os that do not require special setup, hold, or valid requirements. Most of these are asynchronous to the system clock. The following numbers are provided for test and validation purposes only, and they assume a 133 MHz internal bus frequency.

Figure 45 shows the GPIO Timing Diagram. Table 50 gives the timing specifications.

Table 50. Asynchronous Signals

| Sym | Description | Min | Max | Units | SpecID |
|----------|--------------|------|-------|-------|--------|
| t_{CK} | Clock Period | 7.52 | — | ns | A16.1 |
| t_{IS} | Input Setup | 12 | — | ns | A16.2 |
| t_{IH} | Input Hold | 1 | — | ns | A16.3 |
| t_{DV} | Output Valid | — | 15.33 | ns | A16.4 |
| t_{DH} | Output Hold | 1 | — | ns | A16.5 |

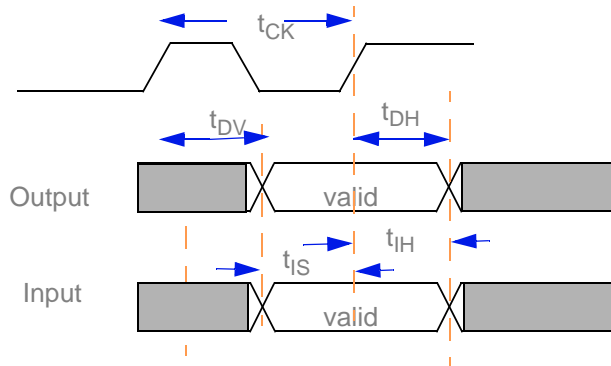


Figure 45. Timing Diagram—Asynchronous Signals

1.3.18 IEEE 1149.1 (JTAG) AC Specifications

Table 51. JTAG Timing Specification

| Sym | Characteristic | Min | Max | Unit | SpecID |
|-----|--|------|-----|------|--------|
| — | TCK frequency of operation. | 0 | 25 | MHz | A17.1 |
| 1 | TCK cycle time. | 40 | — | ns | A17.2 |
| 2 | TCK clock pulse width measured at 1.5V. | 1.08 | — | ns | A17.3 |
| 3 | TCK rise and fall times. | 0 | 3 | ns | A17.4 |
| 4 | $\overline{\text{TRST}}$ setup time to tck falling edge ⁽¹⁾ . | 10 | — | ns | A17.5 |
| 5 | $\overline{\text{TRST}}$ assert time. | 5 | — | ns | A17.6 |
| 6 | Input data setup time ⁽²⁾ . | 5 | — | ns | A17.7 |
| 7 | Input data hold time ⁽²⁾ . | 15 | — | ns | A17.8 |
| 8 | TCK to output data valid ⁽³⁾ . | 0 | 30 | ns | A17.9 |
| 9 | TCK to output high impedance ⁽³⁾ . | 0 | 30 | ns | A17.10 |
| 10 | TMS, TDI data setup time. | 5 | — | ns | A17.11 |
| 11 | TMS, TDI data hold time. | 1 | — | ns | A17.12 |
| 12 | TCK to TDO data valid. | 0 | 15 | ns | A17.13 |
| 13 | TCK to TDO high impedance. | 0 | 15 | ns | A17.14 |

¹ $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

² Non-test, other than TDI and TMS, signal input timing with respect to TCK.

³ Non-test, other than TDO, signal output timing with respect to TCK.

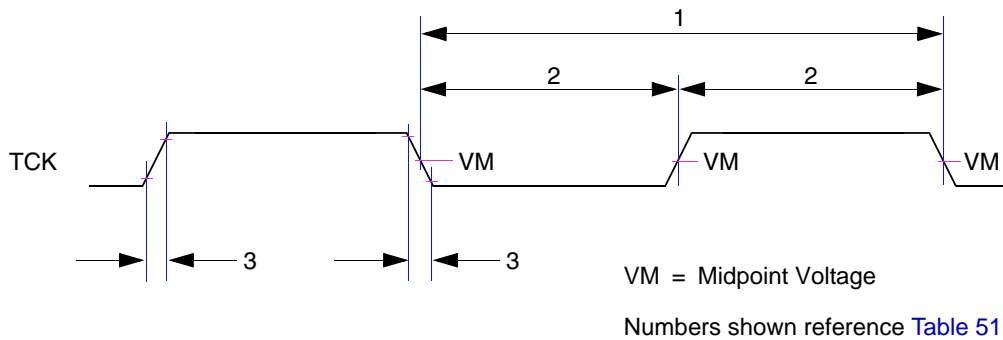


Figure 46. Timing Diagram—JTAG Clock Input

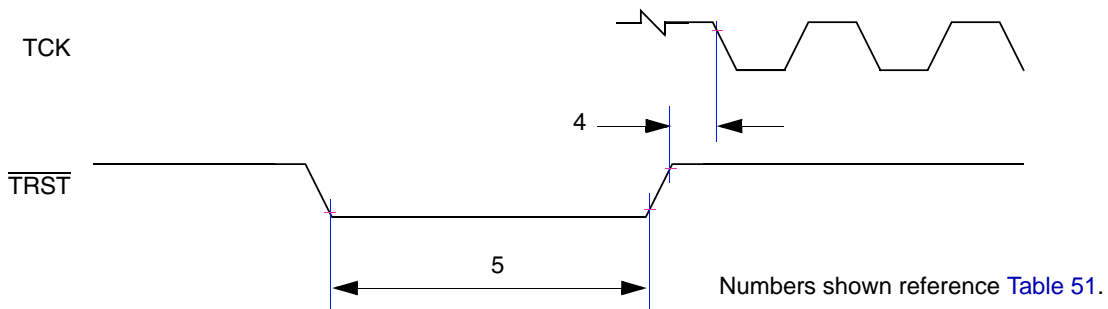


Figure 47. Timing Diagram—JTAG TRST

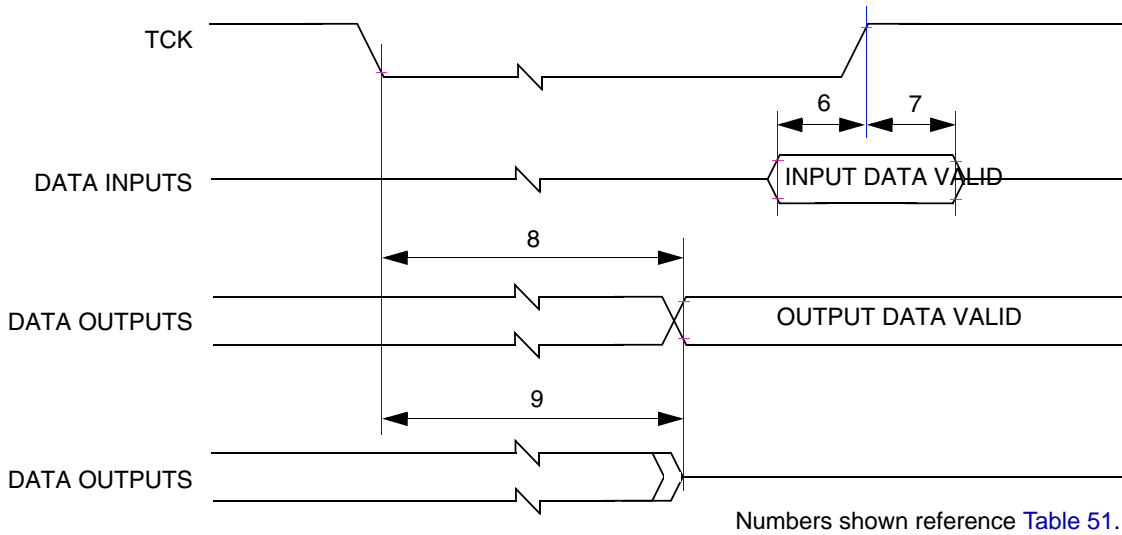


Figure 48. Timing Diagram—JTAG Boundary Scan

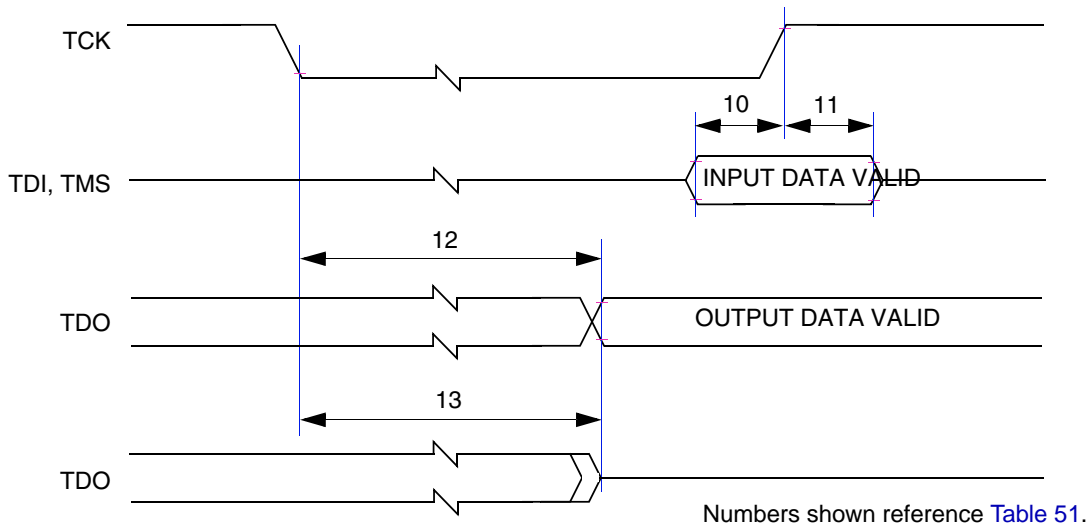


Figure 49. Timing Diagram—Test Access Port

2 Package Description

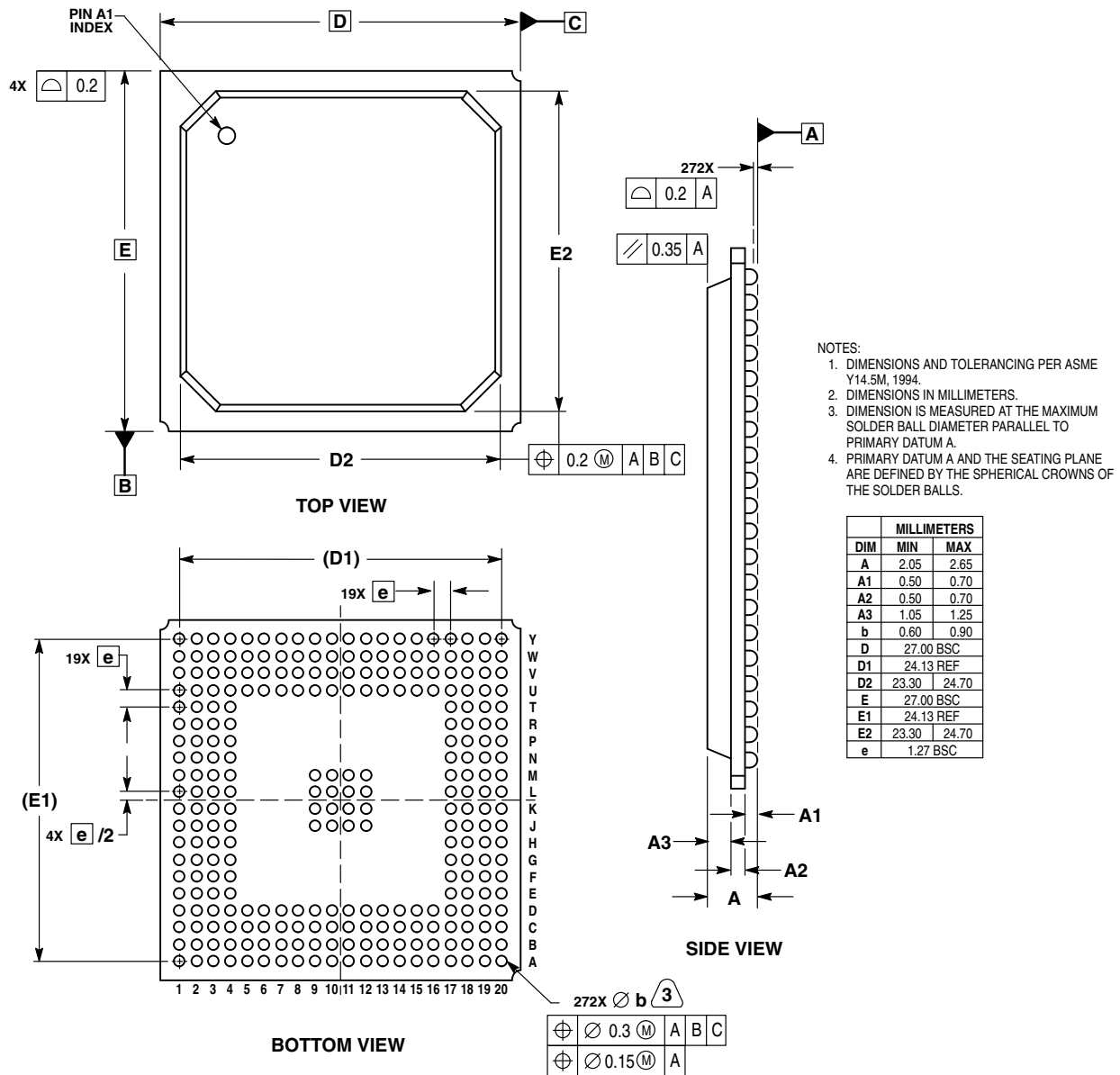
2.1 Package Parameters

The MPC5200B uses a 27 mm x 27 mm TE-PBGA package. The package parameters are as provided in the following list:

- Package outline: 27 mm x 27 mm
- Interconnects: 2
- Pitch: 1.27 mm

2.2 Mechanical Dimensions

Figure 50 provides the mechanical dimensions, top surface, side profile, and pinout for the MPC5200B, 272 TE-PBGA package.



CASE 1135A-01
ISSUE B

Figure 50. Mechanical Dimensions and Pinout Assignments for the MPC5200B, 272 TE-PBGA

2.3 Pinout Listings

See details in the MPC5200B User Manual.

Table 52. MPC5200B Pinout Listing

| Name | Alias | Type | Power Supply | Output Driver Type | Input Type | Pull-up/down |
|------------------------------|--------|------|--------------|--------------------|------------|--------------|
| SDRAM | | | | | | |
| $\overline{\text{MEM_CAS}}$ | CAS | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| MEM_CLK_EN | CLK_EN | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| $\overline{\text{MEM_CS}}$ | | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| MEM_DQM[3:0] | DQM | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| MEM_MA[12:0] | MA | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| MEM_MBA[1:0] | MBA | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| MEM_MDQS[3:0] | MDQS | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| MEM_MDQ[31:0] | MDQ | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| MEM_CLK | | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| MEM_CLK | | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| $\overline{\text{MEM_RAS}}$ | RAS | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| $\overline{\text{MEM_WE}}$ | | I/O | VDD_MEM_IO | DRV16_MEM | TTL | |
| PCI | | | | | | |
| EXT_AD[31:0] | | I/O | VDD_IO | PCI | PCI | |
| PCI_CBE_0 | | I/O | VDD_IO | PCI | PCI | |
| PCI_CBE_1 | | I/O | VDD_IO | PCI | PCI | |
| PCI_CBE_2 | | I/O | VDD_IO | PCI | PCI | |
| PCI_CBE_3 | | I/O | VDD_IO | PCI | PCI | |
| PCI_CLOCK | | I/O | VDD_IO | PCI | PCI | |
| PCI_DEVSEL | | I/O | VDD_IO | PCI | PCI | |
| PCI_FRAME | | I/O | VDD_IO | PCI | PCI | |
| PCI_GNT | | I/O | VDD_IO | DRV8 | TTL | |
| PCI_IDSEL | | I/O | VDD_IO | DRV8 | TTL | |
| PCI_IRDY | | I/O | VDD_IO | PCI | PCI | |
| PCI_PAR | | I/O | VDD_IO | PCI | PCI | |
| PCI_PERR | | I/O | VDD_IO | PCI | PCI | |
| PCI_REQ | | I/O | VDD_IO | DRV8 | TTL | |
| PCI_RESET | | I/O | VDD_IO | PCI | PCI | |
| PCI_SERR | | I/O | VDD_IO | PCI | PCI | |
| PCI_STOP | | I/O | VDD_IO | PCI | PCI | |

Table 52. MPC5200B Pinout Listing (continued)

| Name | Alias | Type | Power Supply | Output Driver Type | Input Type | Pull-up/down |
|-------------------|-------------------------|------|--------------|--------------------|------------|--------------|
| PCI_TRDY | | I/O | VDD_IO | PCI | PCI | |
| Local Plus | | | | | | |
| LP_ACK | | I/O | VDD_IO | DRV8 | TTL | PULLUP |
| LP_ALE | | I/O | VDD_IO | DRV8 | TTL | |
| LP_OE | | I/O | VDD_IO | DRV8 | TTL | |
| LP_RW | | I/O | VDD_IO | DRV8 | TTL | |
| LP_TS | | I/O | VDD_IO | DRV8 | TTL | |
| LP_CS0 | | I/O | VDD_IO | DRV8 | TTL | |
| LP_CS1 | | I/O | VDD_IO | DRV8 | TTL | |
| LP_CS2 | | I/O | VDD_IO | DRV8 | TTL | |
| LP_CS3 | | I/O | VDD_IO | DRV8 | TTL | |
| LP_CS4 | | I/O | VDD_IO | DRV8 | TTL | |
| LP_CS5 | | I/O | VDD_IO | DRV8 | TTL | |
| ATA | | | | | | |
| ATA_DACK | | I/O | VDD_IO | DRV8 | TTL | |
| ATA_DRQ | | I/O | VDD_IO | DRV8 | TTL | PULLDOWN |
| ATA_INTRQ | | I/O | VDD_IO | DRV8 | TTL | PULLDOWN |
| ATA_IOCHRDY | | I/O | VDD_IO | DRV8 | TTL | PULLUP |
| ATA_IOR | | I/O | VDD_IO | DRV8 | TTL | |
| ATA_IOW | | I/O | VDD_IO | DRV8 | TTL | |
| ATA_ISOLATION | | I/O | VDD_IO | DRV8 | TTL | |
| Ethernet | | | | | | |
| ETH_0 | TX, TX_EN | I/O | VDD_IO | DRV4 | TTL | |
| ETH_1 | RTS, TXD[0] | I/O | VDD_IO | DRV4 | TTL | |
| ETH_2 | USB_TXP, RTX, TXD[1] | I/O | VDD_IO | DRV4 | TTL | |
| ETH_3 | USB_PRTPW, TXD[2] | I/O | VDD_IO | DRV4 | TTL | |
| ETH_4 | USB_SPEED, TXD[3] | I/O | VDD_IO | DRV4 | TTL | |
| ETH_5 | USB_SUPEND, TX_ER | I/O | VDD_IO | DRV4 | TTL | |
| ETH_6 | USB_OE, RTS, MDC | I/O | VDD_IO | DRV4 | TTL | |
| ETH_7 | TXN, MDIO | I/O | VDD_IO | DRV4 | TTL | |

Table 52. MPC5200B Pinout Listing (continued)

| Name | Alias | Type | Power Supply | Output Driver Type | Input Type | Pull-up/down |
|-----------------------|---------------------------|------|--------------|--------------------|------------|--------------|
| ETH_8 | RX_DV | I/O | VDD_IO | DRV4 | TTL | |
| ETH_9 | CD, RX_CLK | I/O | VDD_IO | DRV4 | Schmitt | |
| ETH_10 | CTS, COL | I/O | VDD_IO | DRV4 | TTL | |
| ETH_11 | TX_CLK | I/O | VDD_IO | DRV4 | Schmitt | |
| ETH_12 | RXD[0] | I/O | VDD_IO | DRV4 | TTL | |
| ETH_13 | USB_RXD, CTS, RXD[1] | I/O | VDD_IO | DRV4 | TTL | |
| ETH_14 | USB_RXP, UART_RX, RXD[2] | I/O | VDD_IO | DRV4 | TTL | |
| ETH_15 | USB_RXN, RX, RXD[3] | I/O | VDD_IO | DRV4 | TTL | |
| ETH_16 | USB_OVRCNT, CTS, RX_ER | I/O | VDD_IO | DRV4 | TTL | |
| ETH_17 | CD, CRS | I/O | VDD_IO | DRV4 | TTL | |
| IRDA | | | | | | |
| PSC6_0 | IRDA_RX, RxD | I/O | VDD_IO | DRV4 | TTL | |
| PSC6_1 | Frame, CTS | I/O | VDD_IO | DRV4 | TTL | |
| PSC6_2 | IRDA_TX, TxD | I/O | VDD_IO | DRV4 | TTL | |
| PSC6_3 | IR_USB_CLK, BitClock, RTS | I/O | VDD_IO | DRV4 | Schmitt | |
| USB | | | | | | |
| USB_0 | USB_OE | I/O | VDD_IO | DRV4 | TTL | |
| USB_1 | USB_TXN | I/O | VDD_IO | DRV4 | TTL | |
| USB_2 | USB_TXP | I/O | VDD_IO | DRV4 | TTL | |
| USB_3 | USB_RXD | I/O | VDD_IO | DRV4 | TTL | |
| USB_4 | USB_RXP | I/O | VDD_IO | DRV4 | TTL | |
| USB_5 | USB_RXN | I/O | VDD_IO | DRV4 | TTL | |
| USB_6 | USB_PRT_PWR | I/O | VDD_IO | DRV4 | TTL | |
| USB_7 | USB_SPEED | I/O | VDD_IO | DRV4 | TTL | |
| USB_8 | USB_SUSPEND | I/O | VDD_IO | DRV4 | TTL | |
| USB_9 | USB_OVRCNT | I/O | VDD_IO | DRV4 | TTL | |
| I²C | | | | | | |
| I2C_0 | SCL | I/O | VDD_IO | DRV4 | Schmitt | |
| I2C_1 | SDA | I/O | VDD_IO | DRV4 | Schmitt | |
| I2C_2 | SCL | I/O | VDD_IO | DRV4 | Schmitt | |

Table 52. MPC5200B Pinout Listing (continued)

| Name | Alias | Type | Power Supply | Output Driver Type | Input Type | Pull-up/down |
|-------------------|---------------------------------------|------|--------------|--------------------|------------|--------------|
| I2C_3 | SDA | I/O | VDD_IO | DRV4 | Schmitt | |
| PSC | | | | | | |
| PSC1_0 | TxD, Sdata_out, MOSI, TX | I/O | VDD_IO | DRV4 | TTL | |
| PSC1_1 | RxD, Sdata_in, MISO, TX | I/O | VDD_IO | DRV4 | TTL | |
| PSC1_2 | Mclk, Sync, RTS | I/O | VDD_IO | DRV4 | TTL | |
| PSC1_3 | BitClk, SCK, CTS | I/O | VDD_IO | DRV4 | Schmitt | |
| PSC1_4 | Frame, \overline{SS} , CD | I/O | VDD_IO | DRV4 | TTL | |
| PSC2_0 | TxD, Sdata_out, MOSI, TX | I/O | VDD_IO | DRV4 | TTL | |
| PSC2_1 | RxD, Sdata_in, MISO, TX | I/O | VDD_IO | DRV4 | TTL | |
| PSC2_2 | Mclk, Sync, RTS | I/O | VDD_IO | DRV4 | TTL | |
| PSC2_3 | BitClk, SCK, CTS | I/O | VDD_IO | DRV4 | Schmitt | |
| PSC2_4 | Frame, \overline{SS} , CD | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_0 | USB_OE, TxDS, TX | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_1 | USB_TXN, RxD, RX | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_2 | USB_TXP, BitClk, RTS | I/O | VDD_IO | DRV4 | Schmitt | |
| PSC3_3 | USB_RXD, Frame, \overline{SS} , CTS | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_4 | USB_RXP, CD | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_5 | USB_RXN | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_6 | USB_PRTPWR, Mclk, MOSI | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_7 | USB_SPEED, MISO | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_8 | USB_SUPEND, \overline{SS} | I/O | VDD_IO | DRV4 | TTL | |
| PSC3_9 | USB_OVRCNT, SCK | I/O | VDD_IO | DRV4 | TTL | |
| GPIO/TIMER | | | | | | |
| GPIO_WKUP_6 | MEM_CS1 | I/O | VDD_MEM_IO | DRV16_MEM | TTL | PULLUP_MEM |
| GPIO_WKUP_7 | | I/O | VDD_IO | DRV8 | TTL | |
| TIMER_0 | | I/O | VDD_IO | DRV4 | TTL | |

Table 52. MPC5200B Pinout Listing (continued)

| Name | Alias | Type | Power Supply | Output Driver Type | Input Type | Pull-up/down |
|---------------------------|-------|--------|--------------|----------------------|------------|--------------|
| TIMER_1 | | I/O | VDD_IO | DRV4 | TTL | |
| TIMER_2 | MOSI | I/O | VDD_IO | DRV4 | TTL | |
| TIMER_3 | MISO | I/O | VDD_IO | DRV4 | TTL | |
| TIMER_4 | SS | I/O | VDD_IO | DRV4 | TTL | |
| TIMER_5 | SCK | I/O | VDD_IO | DRV4 | TTL | |
| TIMER_6 | | I/O | VDD_IO | DRV4 | TTL | |
| TIMER_7 | | I/O | VDD_IO | DRV4 | TTL | |
| Clock | | | | | | |
| SYS_XTAL_IN | | Input | VDD_IO | | | |
| SYS_XTAL_OUT | | Output | VDD_IO | | | |
| RTC_XTAL_IN | | Input | VDD_IO | | | |
| RTC_XTAL_OUT | | Output | VDD_IO | | | |
| Misc | | | | | | |
| PORRESET | | Input | VDD_IO | DRV4 | Schmitt | |
| HRESET | | I/O | VDD_IO | DRV8_OD ¹ | Schmitt | |
| SRESET | | I/O | VDD_IO | DRV8_OD ¹ | Schmitt | |
| IRQ0 | | I/O | VDD_IO | DRV4 | TTL | |
| IRQ1 | | I/O | VDD_IO | DRV4 | TTL | |
| IRQ2 | | I/O | VDD_IO | DRV4 | TTL | |
| IRQ3 | | I/O | VDD_IO | DRV4 | TTL | |
| Test/Configuration | | | | | | |
| SYS_PLL_TPA | | I/O | VDD_IO | DRV4 | TTL | |
| TEST_MODE_0 | | Input | VDD_IO | DRV4 | TTL | |
| TEST_MODE_1 | | Input | VDD_IO | DRV4 | TTL | |
| TEST_SEL_0 | | I/O | VDD_IO | DRV4 | TTL | PULLUP |
| TEST_SEL_1 | | I/O | VDD_IO | DRV8 | TTL | |
| JTAG_TCK | TCK | Input | VDD_IO | DRV4 | Schmitt | PULLUP |
| JTAG_TDI | TDI | Input | VDD_IO | DRV4 | TTL | PULLUP |
| JTAG_TDO | TDO | I/O | VDD_IO | DRV8 | TTL | |
| JTAG_TMS | TMS | Input | VDD_IO | DRV4 | TTL | PULLUP |
| JTAG_TRST | TRST | Input | VDD_IO | DRV4 | TTL | PULLUP |
| Power and Ground | | | | | | |
| VDD_IO | | - | | | | |

Table 52. MPC5200B Pinout Listing (continued)

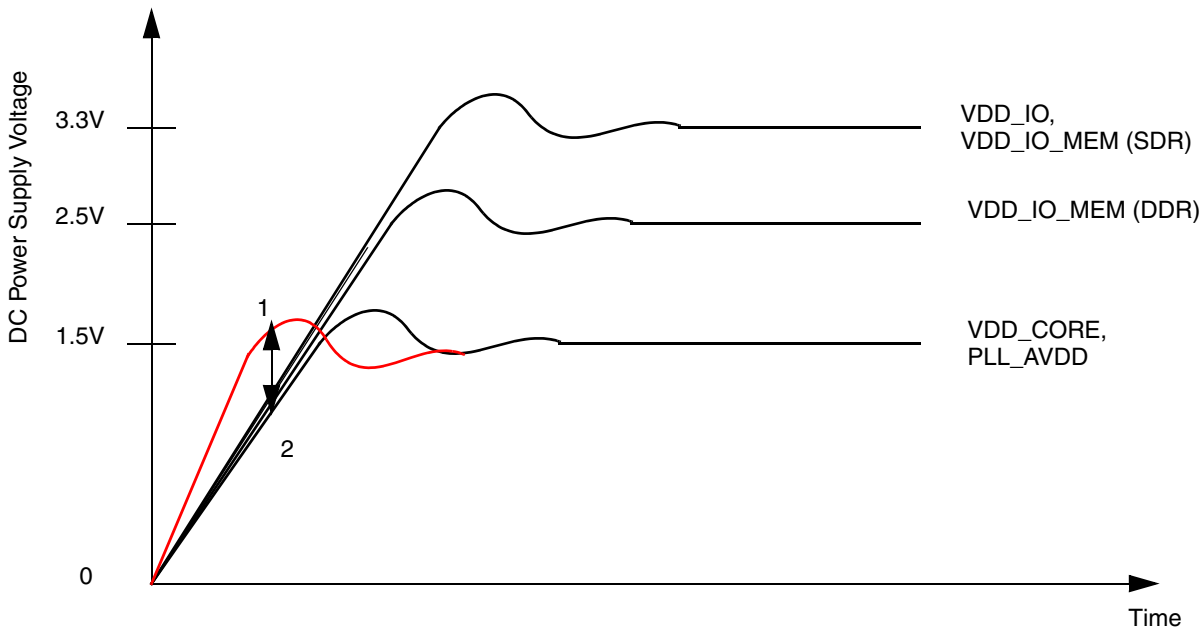
| Name | Alias | Type | Power Supply | Output Driver Type | Input Type | Pull-up/down |
|---------------|-------|------|--------------|--------------------|------------|--------------|
| VDD_MEM_IO | | - | | | | |
| VDD_CORE | | - | | | | |
| VSS_IO/CORE | | - | | | | |
| SYS_PLL_AVDD | | - | | | | |
| CORE_PLL_AVDD | | - | | | | |

¹ All “open drain” outputs of the MPC5200B are actually regular three-state output drivers with the output data tied low and the output enable controlled. Thus, unlike a true open drain, there is a current path from the external system to the MPC5200B I/O power rail if the external signal is driven above the MPC5200B I/O power rail voltage.

3 System Design Information

3.1 Power Up/Down Sequencing

Figure 51 shows situations in sequencing the I/O VDD (VDD_IO), Memory VDD (VDD_IO_MEM), PLL VDD (PLL_AVDD), and Core VDD (VDD_CORE).



Note: VDD_CORE should not exceed VDD_IO, VDD_IO_MEM or PLL_AVDD by more than 0.4 V at any time, including power-up.

Note: It is recommended that VDD_CORE/PLL_AVDD should track VDD_IO/VDD_IO_MEM up to 0.9 V then separate for completion of ramps.

Note: Input voltage must not be greater than the supply voltage (VDD_IO) VDD_IO_MEM, VDD_CORE, or PLL_AVDD) by more than 0.5 V at any time, including during power-up.

Note: Use 1 microsecond or slower rise time for all supplies.

Figure 51. Supply Voltage Sequencing

The relationship between VDD_IO_MEM and VDD_IO is non-critical during power-up and power-down sequences. VDD_IO_MEM (2.5 V or 3.3 V) and VDD_IO are specified relative to VDD_CORE.

3.1.1 Power Up Sequence

If VDD_IO/VDD_IO_MEM are powered up with the VDD_CORE at 0V, the sense circuits in the I/O pads cause all pad output drivers connected to the VDD_IO/VDD_IO_MEM to be in a high-impedance state. There is no limit to how long after VDD_IO/VDD_IO_MEM powers up before VDD_CORE must power up. VDD_CORE should not lead the VDD_IO, VDD_IO_MEM or PLL_AVDD by more than 0.4 V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

Use one microsecond or slower rise time for all supplies.

VDD_CORE/PLL_AVDD and VDD_IO/VDD_IO_MEM should track up to 0.9 V and then separate for the completion of ramps with VDD_IO/VDD_IO_MEM going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

3.1.2 Power Down Sequence

If VDD_CORE/PLL_AVDD are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after VDD_CORE and PLL_AVDD power down before VDD_IO or VDD_IO_MEM must power down. VDD_CORE should not lag VDD_IO, VDD_IO_MEM, or PLL_AVDD going low by more than 0.5V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop VDD_CORE/PLL_AVDD to 0V.
2. Drop VDD_IO/VDD_IO_MEM supplies.

3.2 System and CPU Core AVDD Power Supply Filtering

Each of the independent PLL power supplies require filtering external to the device. The following drawing is a recommendation for the required filter circuit.

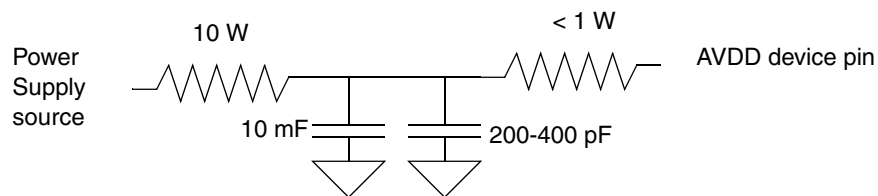


Figure 52. Power Supply Filtering

3.3 Pull-up/Pull-down Resistor Requirements

The MPC5200B requires external pull-up or pull-down resistors on certain pins.

3.3.1 Pull-down Resistor Requirements for TEST pins

The MPC5200B requires pull-down resistors on the test pins TEST_MODE_0, TEST_MODE_1, TEST_SEL_1.

3.3.2 Pull-up Requirements for the PCI Control Lines

If the PCI interface is NOT used (and internally disabled) the PCI control pins must be terminated as indicated by the PCI Local Bus specification. This is also required for MOST/Graphics and Large Flash Mode.

PCI control signals always require pull-up resistors on the motherboard (not the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes PCI_FRAME, PCI_TRDY, PCI_IRDY, PCI_DEVSEL, PCI_STOP, PCI_SERR, PCI_PERR, and PCI_REQ.

3.3.3 Pull-up/Pull-down Requirements for MEM_MDQS Pins (SDRAM)

The MEM_MDQS[3:0] signals are not used with SDR memories and require pull-up or pull-down resistors in SDRAM mode.

3.3.4 Pull-up/Pull-down Requirements for MEM_MDQS Pins (DDR 16-bit Mode)

The MEM_MDQS[1:0] signals are not used in DDR 16-bit mode and require pull-down resistors.

3.4 JTAG

The MPC5200B provides the user an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a Common On-Chip Processor (COP) Interface, which shares the IEEE 1149.1 JTAG port. The COP Interface provides access to the MPC5200B's embedded Freescale (formerly Motorola) MPC603e e300 processor. This interface provides a means for executing test routines and for performing software development and debug functions.

3.4.1 JTAG_TRST

Boundary scan testing is enabled through the JTAG interface signals. The JTAG_TRST signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the PowerPC architecture. To obtain a reliable power-on reset performance, the JTAG_TRST signal must be asserted during power-on reset.

3.4.1.1 JTAG_TRST and PORRESET

The JTAG interface can control the direction of the MPC5200B I/O pads via the boundary scan chain. The JTAG module must be reset before the MPC5200B comes out of power-on reset; do this by asserting JTAG_TRST before PORRESET is released.

For more details refer to the Reset and JTAG Timing Specification.

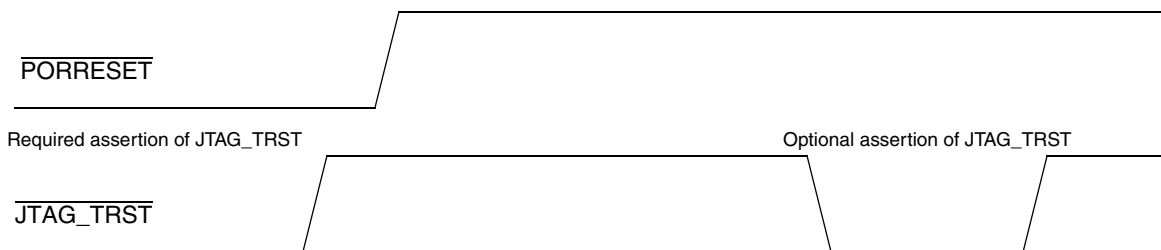


Figure 53. $\overline{\text{PORRESET}}$ vs. $\overline{\text{JTAG_TRST}}$

3.4.1.2 Connecting JTAG_TRST

The wiring of the $\overline{\text{JTAG_TRST}}$ depends on the existence of a board-related debug interface. (see below)

Normally this interface is implemented, using a COP (common on-chip processor) connector. The COP allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the MPC5200B.

3.4.2 e300 COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

3.4.2.1 Boards Interfacing the JTAG Port via a COP Connector

The MPC5200B functional pin interface and internal logic provides access to the embedded e300 processor core through the Freescale (formerly Motorola) standard COP/BDM interface. [Table 53](#) gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

| BDM Pin # | MPC5200B I/O Pin | BDM Connector | Internal Pull Up/Down | External Pull Up/Down | I/O ¹ |
|-----------|------------------|---------------------|-----------------------|-----------------------|------------------|
| 16 | — | GND | — | — | — |
| 15 | TEST_SEL_0 | ckstp_out | — | — | I |
| 14 | — | KEY | — | — | — |
| 13 | HRESET | hreset | — | 10k Pull-Up | O |
| 12 | — | GND | — | — | — |
| 11 | SRESET | sreset | — | 10k Pull-Up | O |
| 10 | — | N/C | — | — | — |
| 9 | JTAG_TMS | tms | 100k Pull-Up | 10k Pull-Up | O |
| 8 | — | N/C | — | — | — |
| 7 | JTAG_TCK | tck | 100k Pull-Up | 10k Pull-Up | O |
| 6 | — | VDD ² | — | — | — |
| 5 | — | halted ³ | — | — | I |
| 4 | JTAG_TRST | trst | 100k Pull-Up | 10k Pull-Up | O |
| 3 | JTAG_TDI | tdi | 100k Pull-Up | 10k Pull-Up | O |
| 2 | — | qack ⁴ | — | — | O |
| 1 | JTAG_TDO | tdo | — | — | I |

¹ With respect to the emulator tool's perspective, Input is really an output from the embedded e300 core and output is really an input to the core.

² From the board under test, power sense for chip power.

³ HALTED is not available from e300 core.

⁴ Input to the e300 core to enable/disable soft-stop condition during breakpoints. MPC5200B internally ties CORE_QACK to GND in its normal/functional mode (always asserted).

For a board with a COP (common on-chip processor) connector, which accesses the JTAG interface and which needs to reset the JTAG module, simply wiring JTAG_TRST and PORRESET is not recommended.

To reset the MPC5200B via the COP connector, the $\overline{\text{HRESET}}$ pin of the COP should be connected to the $\overline{\text{HRESET}}$ pin of the MPC5200B. The circuitry shown in Figure 54 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{JTAG_TRST}}$ separately, while any other board sources can drive $\overline{\text{PORRESET}}$.

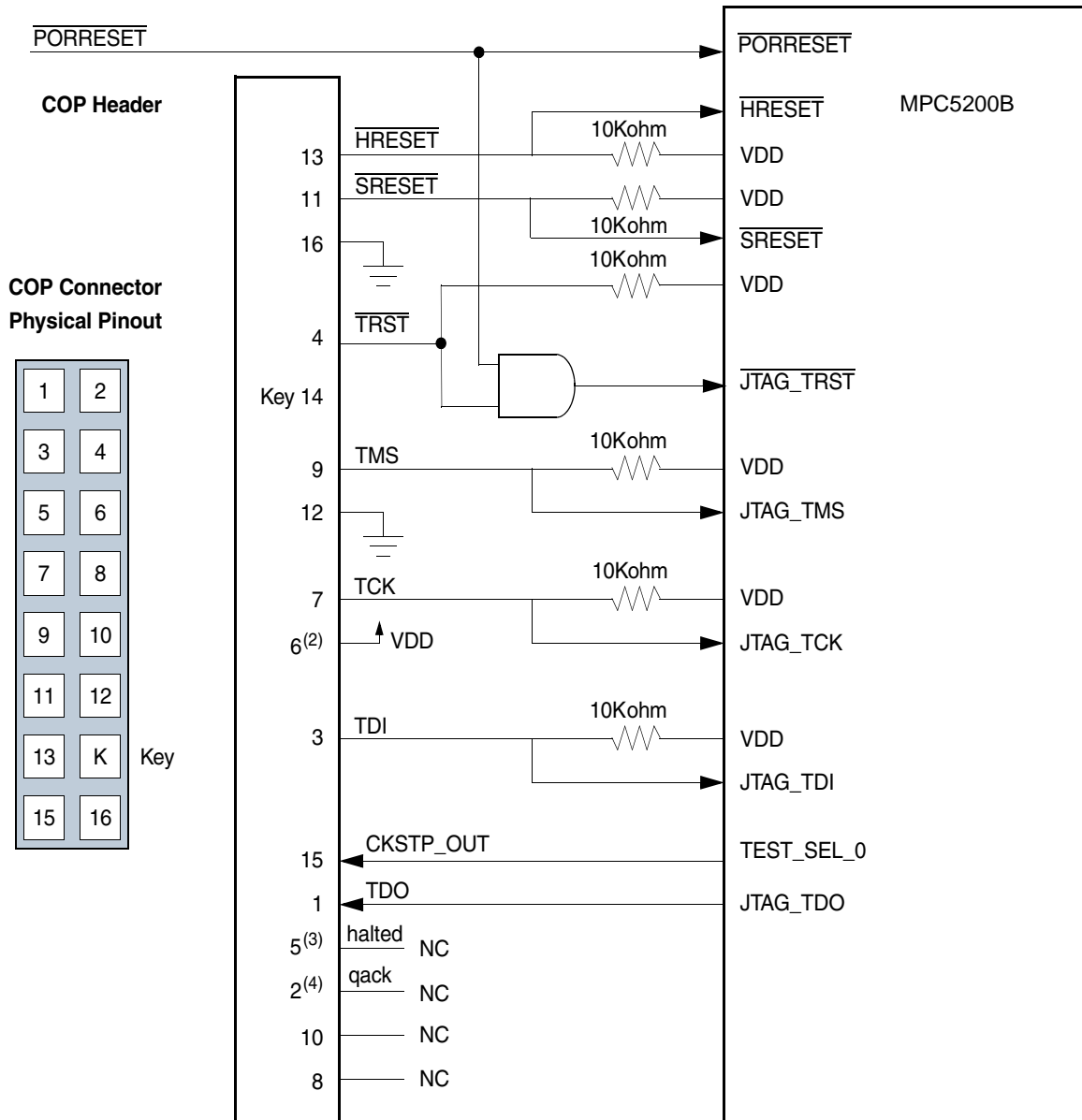


Figure 54. COP Connector Diagram

3.4.2.2 Boards Without COP Connector

If the JTAG interface is not used, $\overline{\text{JTAG_TRST}}$ should be tied to $\overline{\text{PORRESET}}$, so that it is asserted when the system reset signal ($\overline{\text{PORRESET}}$) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 55 shows the connection of the JTAG interface without COP connector.

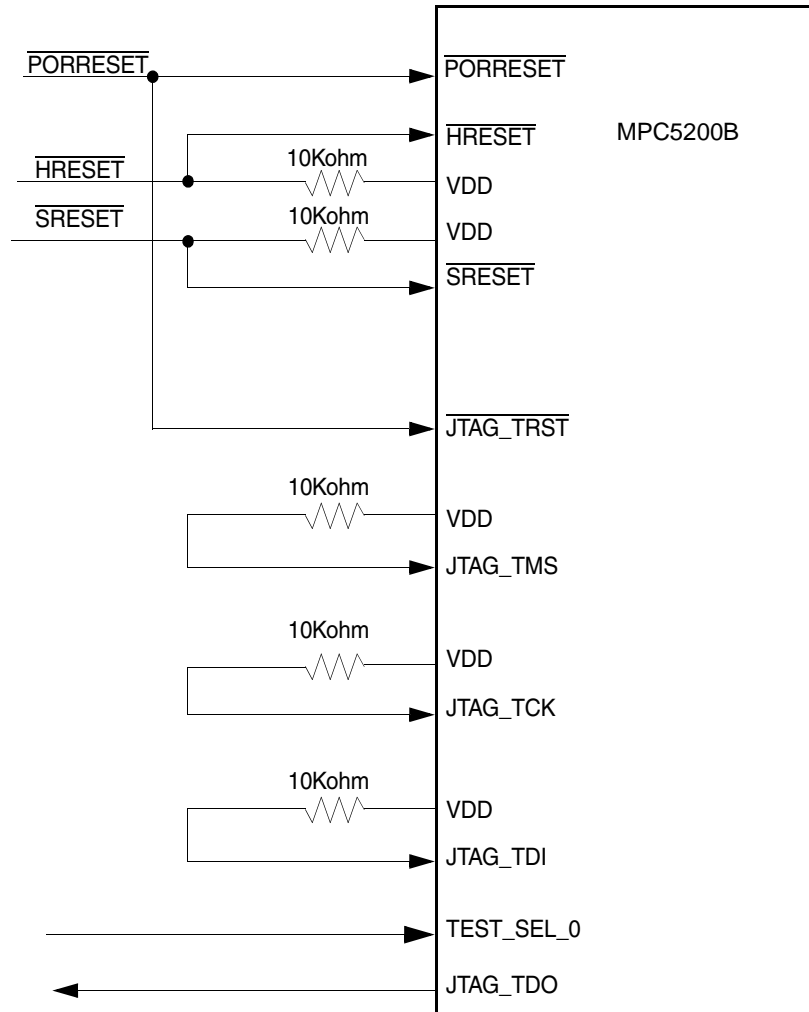


Figure 55. $\overline{\text{JTAG_TRST}}$ Wiring for Boards without COP Connector

4 Ordering Information

Table 54. Ordering Information

| Part Number ¹ | Speed | Ambient Temp | Qualification ² | Packaging ³ |
|--------------------------|-------|--------------|----------------------------|------------------------|
| MPC5200VR400B | 400 | 0C to 70C | Commercial | RoHS & pb-free |
| MPC5200CVR466B | 400 | -40C to 85C | Industrial | RoHS & pb-free |
| SPC5200VVR266B | 266 | -40C to 105C | Automotive – AEC | RoHS & pb-free |
| SPC5200CBV400B | 400 | -40C to 85C | Automotive – AEC | Standard |
| SPC5200CVR400B | 400 | -40C to 85C | Automotive – AEC | RoHS & pb-free |

¹ Shipped in trays. Add “R2” suffix for Tape & Reel.

² Commercial Qualified to <250PPM level. Industrial/Automotive Qualified to AEC-Q100. Automotive has Zero Defect flow.

³ Standard is halide-free with pb solder balls.

5 Document Revision History

Table 55 provides a revision history for this hardware specification.

Table 55. Document Revision History

| Rev. No. | Differences |
|-----------------|---|
| 1 | Clock Frequencies table: 466 MHz was changed to 400 MHz for the e300 Processor Core |
| 2 | Added description for PCI CLK Slew Rate for PCI CLK Specifications table. |
| | Added description for minimum rates in the DDR SDRAM Memory Write Timing table. |
| 3 | Added one item to table "DDR SDRAM Memory Read Timing." |



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